SOLID-STATE MICROWAVE AMPLIFICATION INTO MILLIMETRIC FREQUENCIES for consideration of PhD by published works

C.H.Oxley

A thesis submitted in partial fulfillment of the requirements for the degree of Doctor of Philosophy

De Montfort University

May 2005

KEY WORDS:

TRAPATT (trapped avalanche plasma trigger transit) diode
MESFET (Metal semiconductor field effect transistor)
HEMT (High electron mobility transistor)
LGT (Linear gate transistor)
TWF (Travelling wave field effect transistor)
TWA (Travelling wave amplifier)
NF_{min} (Minimum noise figure)
S-parameters (scattering parameters)
GaAs (Gallium arsenide)
GaN (Gallium nitride)
AlGaN (Aluminum gallium nitride)
AlGaAs (Aluminum gallium arsenide)

Declaration

This dissertation contains the results of research undertaken by myself, between 1975 and February 2004. To assist the reader, the research work presented in this thesis has been split into three distinct periods. During the first (1975 to 1979) and second period (1980 to 1987), the work was carried out at the Allen Clark Research Centre, Caswell, UK. The third period (2000 to 2004) the work was carried out at De Montfort University. The research work is presented in the form of published papers under the supervision of Prof. E .M. Shankara Narayanan, De Montfort University.

This work is the outcome of my research and nothing is done under collaboration except where stated or indicated. To the best of my knowledge, the contents of this dissertation have not been submitted as a whole, or in part for any degree or diploma at any other academic institution.

Permission is hereby granted to consult or copy information contained herein for the purpose of private study but not for any other purpose.

Christopher H. Oxley
De Montfort University,
Leicester,
LE1 9BH,
UK.
e-mail choxley@dmu.ac.uk

ABSTRACT

The work presented in this thesis is published research work undertaken by the author over a long period of time 1975 to 2004, and to assist the reader it is split into three periods. The first period covers 1975 to 1979 and concentrates on the research and development of the silicon TRAPATT diode for use in an X-band power amplifier suitable for airborne application. The work includes the development and measurement of the thermal operation of the diode, the microwave circuit design required for the class - C reflection amplifier operation and an in depth analysis of the technical problems associated with the design of high-frequency TRAPATT circuits, which final led to the decline of the technology at frequencies beyond S-band.

The second period covers 1980 to 1987 and describes in detail the authors' contribution in the development of a milli-metric GaAs MESFET giving state of the art minimum noise performance in the mid 1980's. The work covers research into the design aspects of the transistor, and in particular the RF characterization and the development of an equivalent circuit model. The minimum noise figure measurements were compared with Fukui model and deviation at the high frequency was identified and was attributed to distributed effects along the electrode metallization patterns. The work also led to the invention of a new travelling wave structure, the LGT (linear gate transistor) which was fabricated and fully RF characterized. The work describes the LGT structure in detail which was ahead of its time with respect to the available technology for fabrication.

The third period covers 2000 to 2004 where the author extended his research work into microwave transistors fabricated on wide band-gap materials, for example Gallium Nitride (GaN). The work includes noise analysis of the GaN high electron mobility transistor (HEMT) using the Fukui analysis. The prime part of the work has been in extracting the intrinsic device parameters over bias conditions, which has led to novel method of extracting the parasitic source resistance (R_s) and the intrinsic saturation velocity (v_{si}). The extracted intrinsic parameters are used for both large signal and minimum noise analysis.

DEDICATION

I would like to dedicate this work to my late wife Barbara who gave me three wonderful children (Georgina, Philippa, and Matthew) and enormous encouragement during the years where the majority of this work was undertaken at the Allen Clark Research Centre. In more recent years I would like also to remember my younger daughter Hannah.

ACKNOWLEDGEMENTS

I would like to thank many colleagues at Plessey Research, Caswell who were part of the very successful microwave device and circuits departments led by Dr Jim Turner OBE and Dr Fred Myers respectively, and Dr A J Holden, the co-author of a number of papers (see Appendix 4). I also thank De Montfort University for the opportunity of submitting this thesis.

I wish also to thank my parents for their continued support and in particular my father T. H .Oxley for proof reading the thesis. I am also grateful to Prof E. M. Shankara Narayanan for his corrections and help in suggesting the layout of the thesis and Dr. A. Duffy for his continued encouragement.

I would also like to thank the IEE, IEEE, Elsevier and Microwave Engineering Europe for permission to re-print copies of the papers included in the appendix 6 of the thesis.

CONTENTS

KEYWORDS

DECLARATION

ABSTRACT

DEDICATION

ACKNOWLEDGEMENTS

PRESENTED PUBLISHED PAPERS

Introduction

Period 1: The TRAPATT

Period 2: The GaAs MESFET

Period 3: Wide Band-Gap High Electron Mobility Transistors (HEMTs)

CHAPTER 1: INTRODUCTION

1.1 Solid State Microwave Generators

1.2 Microwave Device Background

1.2.1 Energy Bands

1.2.2 Semiconductor doping

1.2.3 Carrier Transport and Conductivity

1.2.4 Drift Velocity and Mobility

1.2.5 Impact Ionization and Avalanche Mutiplication

1.2.6 Contact Properties

1.2.6.1 Ohmic Contacts

1.2.6.2 The p-n junction

1.2.6.3 Capacitive Nature of the p-n junction

1.2.7 The Metal Semiconductor Field Effect Transistor (MESFET)

1.2.8 The High Electron Mobility Transistor (HEMT)

1.2.9 Reverse bias p-n junctions – the IMPATT and TRAPATT diodes

1.3 Rational for studying

CHAPTER 2: HIGH POWER MICROWAVE AMPLIFIER for I-BAND

2.1 Introduction

2.2 Reflection Amplifiers

2.3 TRAPATT mode

2.4 Target Specification for I-Band TRAPATT Amplifier

2.5 TRAPATT Device Operation, Design and Fabrication

2.6 Thermal Design

2.7 Circuit Design

2.8 Amplifier Performance

2.9 Conclusions

CHAPTER 3: THE GALLIUM ARSENIDE METAL SEMICONDUCTOR TRANSISTOR MESFET

3.1 Introduction

3.2 Transistor Design

3.2.1 Source Inductance

3.2.2 Source Resistance

3.2.3 Gate Resistance

3.2.4 Transconductance

3.3 Device Models

3.3.1 DC characterisation

3.4 RF Assessment and Performance of the Transistor

3.4.1 Low Frequency Measurements

3.5 Transistor Device Models

3.5.1 Equivalent Circuit Lumped Element Models
3.5.2 Distributed Circuit Model
3.5.3 Noise Figure Model
3.6 High Frequency Measurements
3.6.1 High Frequency s-Parameters
3.6.2 High Frequency Gain and Minimum Noise Measurement.
3.7 Conclusions

CHAPTER 4: TRAVELLING WAVE STRUCTURES

4.1 Introduction
4.2.1 Travelling Wave Operation
4.2.2 Travelling Wave FET (TWF)
4.3 Computer Model
4.4 Design of Travelling Wave FET
4.5 Linear Gate Transistor (LGT)
4.5.1 RF Characterisation
4.5.2 Output Power
4.5.3 The third order intermodulation product
4.5.4 Noise performance
4.6 Conclusions
4.7 Recommendations

CHAPTER 5: WIDE BAND-GAP SEMICONDUCTORS

5.1 Introduction

5.2 Development of a small signal equivalent circuit model

5.3 Noise performance of a GaN HEMT

5.4 A more complete analytical noise model for GaN devices.

CHAPTER 6: CONCLUSIONS

CHAPTER 7: FUTURE WORK

REFERENCES

8.1 Published references

8.2 INDUSTRIAL INTERNAL REPORTS giving further evidence of work carried out by the author. These will be identified in the text with the letter I, followed by the reference nos.

9.0 APPENDIX 1: CITATIONS FOR SECTION A

10.0 APPENDIX 2: CITATION FOR SECTION B

11.0 APPENDIX 3: CITATIONS FOR SECTION C.

12.0 APPENDIX 4: Letter form Dr. A. J. Holden confirming the authors' contribution to the research work presented in this thesis.

13.0 APPENDIX 5: C.H.Oxley & A.J.Holden 'Travelling-wave field-effect transistor patent GB2156152A

12.0 APPENDIX 6: PUBLISHED PAPERS

PRESENTED PUBLISHED PAPERS

Introduction

The published papers presented cover a long period of time from 1975 to 2004. To assist the reader the research work is split into the three distinct periods.

The work presented in the first two periods' covers internationally recognised research on the TRAPATT diode and the GaAs MESFET carried out by the author and submitted as published papers (see appendix 6). The third period covers work on the HEMT, which has been fabricated on wide band-gap semiconductor materials for example Gallium Nitride (GaN). Again the research work has been submitted as published papers (see appendix 6).

In section 8.2 there is a list of the research reports completely or partially prepared by the author, covering Periods 1 and 2 at the Allen Clarke Research Centre, to provide further evidence of the research work carried out by the author. The references will be denoted by the letter **[I]** if used in the text.

Period 1: The TRAPATT

World leading research was undertaken to determine the upper frequency capability of the TRAPATT mode and the feasibility of using the TRAPATT diode in a REFLECTION power amplifier configuration, running from a low voltage source which would be suitable for airborne pulsed radar application. The work has been published in a number of journals and those submitted with the thesis are included in APPENDIX 6, along with a list of citations in APPENDIX 1:

Reference to these published works in the text will be denoted by 'A' for example [A1]

1) C.H.Oxley, A.M.Howard and J.J.Purcell 'Design and Performance of I-Band (8-10GH_z) TRAPATT Diodes and Amplifiers' IEEE Trans MTT-27, nos.5, May 1979.

2) *C.H.Oxley, T.J.Brazil, J.J.Purcell and R.Genner 'The design and performance of J-band ferrite microstrip circulators' Proc.Inst.Elec.Eng, vol 125, nos 8, pp 724-727, Aug 1978.

3) *C.H.Oxley, A.M.Howard and J.J.Purcell 'X-band TRAPATT amplifiers', Electron Letters, vol. 14, pp 416-418, 1977.

4) *C.H.Oxley, A.M.Howard, S.M.R.Gordon, and J.J.Purcell 'High efficiency X-band TRAPATT amplifiers and oscillators' Proc. 6th EMC, Rome, pp 311-315, 1976. Author presented the paper.

5) *C.H.Oxley, A.M.Howard and J.J.Purcell 'Design and performance of TRAPATT devices, oscillators and amplifiers' IEE SSED, vol.1, nos. 1, pp 24-30, 1976. {The paper was an invited paper for the first edition of the SSED).

6) C.H.Oxley 'Rugged Coaxial Microwave Cavity' Submission of invention 16/12/76.

Non first authored papers containing further research work carried out by the author:

7) M.W.Geen, T.J.Brazil and C.H.Oxley 'Locked oscillator power-combining, through a Wilkinson Coupler' IEE Proc H, Vol 129, April 1982, pp 77-82.

The submitted published papers were written between 1975 and 1979, and show the feasibility of operating the TRAPATT diode into J-band and the diode and circuit design required to operate a three-stage power amplifier into X-band. To the authors' knowledge this is still the most complete publication showing an experimental X-band three-stage power TRAPATT amplifier working in class-C. This period will be summarised by showing how the rapid development of the GaAs power MESFET superceded the TRAPATT diode and other two terminal solid-state sources in X and J band.

Period 2: The GaAs MESFET

The author's research work on the GaAs MESFET will cover the period from 1980 to 1987. During this period, pioneering work was carried out to move the f_t of the transistor into the milli-metric frequency range. Devices were designed and fabricated with a f_t in excess of $50GH_z$, and the measured minimum noise figure (NF_{min}) approached 2.2dB at

33GH_z, which represented one of the lowest published measured NF_{min} figures in the early '80's. During this period the GaAs microwave MESFET was seen as a suitable device for a range of applications including wide-band, low noise, and medium power amplification for driving travelling wave tube amplifiers (TWTA). The semi-insulating properties of GaAs and the planar construction of the MESFET paved the way to monolithic microwave integrated circuits (MMIC) [16]. This subsequently led to the development of a new wide bandwidth transistor structure known as the LINEAR GATE TRANSISTOR (LGT), which was subject of an international patent **no. GB2156152,** APPENDIX 5. The work was also extended into the design and non-linear modelling requirements of power MESFETs.

The work was published in a number of journals and those submitted with the thesis are include in APPENDIX 6, along with a list of citations in APPENDIX 2 for each of the publications marked with a "*":

Reference to these published works in the text are denoted by the letter B, for example [B1]

1) C.H.Oxley 'Active devices suitable for millimetric wave operation' Colloqium on millimetre operation, IEE, Digest 1986/109, November 1986.
2) *C.H.Oxley and A.J.Holden 'Simple models for high-frequency MESFETs and comparison with experimental results' IEE Proc, Vol.133, Pt. H, Nos 5, Oct 1986.
3) *C.H.Oxley and A.J.Holden 'Modified Fukui model for high frequency MESFETs' Elec. Lett, 22, 1986, 690-692.
4) C.H.Oxley 'In two decades to millimetric wave gallium arsenide FETs', Allen Clark Research Centre Annual Review, 1985, pp 97-104.
5) *C.H.Oxley 'Q-Band (26-40GH_z) 'GaAs FET Single-Stage Amplifier', Electronics Letters, 18th March 1982, Vol.18, Nos 6.
6) C.H.Oxley, J.Arnold and J.Sparrow 'Q-BAND Microstrip Techniques' IEE Colloquium, April 1982.
7) *C.H.Oxley, A.H.Peake, R.H.Bennett, J.Arnold and R.S.Butlin 'Q-BAND (26-40 GH_z) GaAs FETS, Proc IEDM, Washington, 1981.

Non first authored papers containing further research work carried out by the author:

8) *A.J.Holden, B.T.Debney, J.P.King, J.G.Metcalfe and C.H.Oxley 'Matching of GaAs power FETs using a large signal modelling technique' IEE, Proc Pt. H. 133, 1986, pp399-403.

9) *A.J.Holden, I.Davies, P.Medhurst, and C.H.Oxley 'New wideband GaAs travelling wave device: linear gate transistor' Elec.Lett. 22, 1986, pp 777-778.

10) ++I.Davies, D.Brambley, R.Bennett, A.Powell, and C.H.Oxley 'The design and performance in Q-band of 0.3 micron gate-length MESFETs, ESSDERC' 85, Aachen, Germany, 9-12th September 1985.

11) ++M.D.Scott, A.H.Moore, I.Griffith, R.J.M.Griffiths, R.S.Sussmann, C.H.Oxley 'MOCVD Growth of AlInAs/GaInAs MESFET Heterostructures' ESSDERC' 85, Aachen, Germany, 9-12th September 1985.

12) *A.J.Holden, D.R.Daniel, I.Davies, C.H.Oxley and H.D.Rees 'Gallium arsenide travelling wave field-effect transistors' IEEE, ED-32, pp 61-66, 1985.

13) A.J.Holden and C.H.Oxley 'Travelling wave gallium arsenide transistors, Allen Clark Research Centre Annual Review, 1984, pp 89-96.

14) ++*A.J.Holden and C.H.Oxley 'Computer modelling of travelling wave transistors' Proc. Conf. on Simulation of semiconductor devices and processes, Swansea UK, 9th-12th July, pp 319-329.

++ Copies of the papers not included in the text of the thesis.

Period 3: Wide band-gap High Electron Mobility Transistors (HEMTs)

The third period of research has been carried out at De Montfort University from 1999 to the present day. The author has furthered his interest in microwave transistors, and in particular wide band-gap materials, for example Gallium Nitride (GaN). The work has been primarily in de-embedding the equivalent circuit model from s-parameters and minimum noise performance of the transistor. The de-embedding work has led to a novel method for identifying the magnitude of the intrinsic saturation velocity (v_{si}) in the 2 dimensional (2D) electron gas layer and a method for extracting the source resistance

(R_s), under a range of different bias conditions. The noise performance analysis, used an extended form of the Fukui model, and the effect of different bias-settings on the minimum noise performance with respect to frequency was investigated. The Fukui model has indicated that low noise performance may be obtained from these transistors.
The work presented was published in a number of journals and those submitted with the thesis are included in APPENDIX 6, along with a list of citations in APPENDIX 3 for each of the publications marked with a '*':

Reference to these published works in the text is denoted by the letter C, for example [C1]:-

1) ++C.H.Oxley and M.J.Uren 'Measurement of unity gain cut-off frequency and saturation velocity of a GaN HEMT transistor', trans IEEE ED, Feb 2005.
2) C.H.Oxley 'A novel method for measuring the source resistance R_s of a GaN HEMT device over bias conditions (V_{gs}, V_{ds}). Electronics Letters, 4th March 2004, vol.40, no.5, pp344-346.
3) C.H.Oxley 'Gallium Nitride: the promise of high RF power and low microwave noise performance in S and I band'. To be published in Solid State Electronics 2004.
4) C.H.Oxley 'Noise Performance and Applications of Gallium Nitride (GaN) HEMT Transistors' Proc. Wireless Design Conference, London UK, pp 19-22, May 2002.
5) ++C.H.Oxley 'A simple approach including gate leakage for calculating the minimum noise performance of GaN HEMTs' Microwave and Optical Technology Letters, Volume 33, nos. 2, pp113-115, April 2002.
6) *C.H.Oxley 'Calculation of minimum noise figure using the simple Fukui equation for gallium nitride (GaN) HEMTs' Solid State Electron, 45,pp 677-682, 2001.
7) ++C.H.Oxley and O.Buiu 'Comparison of wide band gap and III-V semiconductor devices' Microwave Engineering Europe, vol 7, nos.10 pp, Nov 2001.
8) ++C.H.Oxley, S.Redfern, B.Prime, T.Brown, D.Spencer, D.Dawson, J.Bird, and G.Hilder 'An Automotive 77GH_z Radar Sensor Designed for Volume Manufacture' Conference Proceedings of Telematics Automotive 2000, Volume 1, pages 10 t0 17, April 2000.

[++] Copies of these papers are not included in the text of the thesis

CHAPTER 1: INTRODUCTION

The development of solid state microwave generators has been enormously rapid. Primarily driven by the reduction in volume of the component, (which could be up to one millionth of the volume compared with the vacuum tube technologies), low operating voltages, high frequency performance and integration; leading to the panacea of low cost, high performance and small size components. A large part of the work described in this thesis took place during the peak of component development in the UK, between mid 1970 and mid 1980; which contributed to the demise of the vacuum tube in many applications and facilitated the transition to solid-state microwave devices, with the development of microwave monolithic integrated circuits (mmic). It is true to say that in the early 1980's the microwave device strengths and short comings were not always obvious, but during closing years of the 1980s the microwave transistor had established itself as the versatile solid-state device for future RF, and microwave low noise and medium power applications. The very recent development (1990 – 2003) of the power HEMT on wide-band gap materials, for example gallium nitride (GaN), will now threaten the traditional vacuum tube technology in many high power applications, for example high power radar and microwave ovens.

1.1 Solid State Microwave Generators

The generation of microwave frequencies using semiconductor devices has very rapidly progressed since the conception of obtaining negative resistance from hot electrons in a reverse biased p-n junction, by Schottky in 1954 [1]. This was expanded by Read [2] to the physical requirements of a working device, which is known as an IMPATT (Impact-Avalanche Transit Time) diode. This work was shortly followed by J.B.Gunn 1963 who showed that hot electrons in GaAs produced negative resistance at microwave frequencies by the transfer of electrons from high to low mobility states, these devices are known as Gunn diodes [3]. In the same decade the field-effect transistor was re-invented by William Shockley and the work published in 1952 [4]. Although the origins of the

field-effect transistor go back to around 1925 when Lillienfield first applied for a Canadian, and shortly later USA patent for the device [5].

Both the output power and noise performance are important in the development of many systems, therefore, both these aspects were explored and to a degree determine which microwave device for a particular application.

The practical realisation of the different microwave generation devices followed quickly, with the first practical Read Avalanche diode being fabricated in 1965 [6], which gave low power at low microwave frequencies. Around the same time, research workers at the Bell Telephone Laboratories in the USA showed that high microwave power could be obtained by reverse biasing a silicon computer diode [7]. Since then significant advances have been made in the device technology and in the understanding of the oscillation mechanism. The Read Impatt diode has since been shown to give high microwave power {in excess of 10 watts continuous wave (cw) operation} and can be successfully operated to high microwave frequencies. Whereas, recent work [8] has shown an output power of 0.5μW at 1.9THz can be obtained from a planar GaAs diode, functioning as a tripler.

In 1968 Prager, Chang and Weisbrod [9] experimentally identified a new mode of oscillation when operating a p-n junction in reverse bias. This mode was known as the TRAPATT (Trapped Plasma Avalanche Triggered Transit) mode. It was distinctly different from the IMPATT mode of operation as the oscillation frequency was well below the IMPATT transit-time frequency and the dc to RF efficiency was at least twice that theoretically calculated for the IMPATT diode. The TRAPATT mode can only be operated successfully under pulsed conditions because of the associated high voltages and current densities, which result in very high junction temperatures. At a frequency between 1 to 2 GHz, 1 kilowatt of pulsed output power with an efficiency in excess of 60% [10] was measured making it the first solid state device to deliver in excess of 1kW of RF pulsed power. This made it a natural contender for consideration of the generation of pulsed microwave high power in L through to J band frequencies. It should be remembered that the IMPATT diode oscillator was capable of sustaining cw operation and to high microwave frequencies. Therefore, the two technologies were not seen as competing. The generation of microwaves in the IMPATT and TRAPATT diodes depended on carrier avalanche processes and with large currents, generating both high

levels of shot and thermal noise, and therefore were not seriously pursued for low noise applications [7].

The field-effect transistor was re-invented by William Shockley and the earliest practical FET structure was described around 1952 and consisted of an alloyed p-n junction, which severely limited the performance. In 1969 Middelhoek realised a silicon MESFET with a 1 micron gate-length giving a maximum frequency of oscillation (f_{max}) of 12GHz, which was much higher than for previously known FET structures and comparable with the best f_{max} for the then current state of the art bipolar transistors [11]. In 1965, the first microwave gallium arsenide (GaAs) metal Schottky barrier field-effect transistor (MESFET) was fabricated and measured by J. Turner at the Plessey Company, Allen Clark Research Centre **[B4]**. The transistor had a gate-length in excess of 100 microns and a 0dB gain cut-off frequency (f_t) of the order of tens of MHz, a photograph of one of these early transistors can be seen **[page 1, B4]**. This paved the way for a rapid development of the microwave GaAs field effect transistor. The transistor action was not dependent on hot-electron processes but relatively small channel currents controlled by the gate, resulting in low shot and thermal noise, giving the feasibility of low noise operation. The MESFET was developed by the author and others and was shown that very low noise figures could be obtained at high microwave frequencies (20-40GHz) with useable microwave gain **[B4]**.

In the last 4 decades, enormous strides have been made in all areas of development of the microwave transistor, including an improved understanding of the physical electronic processes, material growth, fabrication, measurement and application. Today, microwave transistors are fabricated on a wide range of materials including gallium arsenide (GaAs), indium phosphide (InP), silicon (Si) and more recently the wide-band gap materials for example gallium nitride (GaN) and silicon carbide (SiC). The experimental f_t of the pseudomorphic high-electron mobility transistor (PHEMT) based on InP, with a gate-length of 25nm has reached 563 GH_z [12]. Recent published work shows the range of microwave performance from a FET device. For example, laboratory InP based PHEMT devices have measured minimum noise figures (NF_{min}) of 0.25 dB at 12 GH_z [13], while an aluminium gallium nitride/gallium nitride (AlGaN/GaN) HEMT [14] has been

reported with a CW output power in excess of 1000W at $2GH_z$. More recently, Nov 2003, output power densities in excess of 32W/mm at 8GHz [15] was reported for a AlGaN/GaN HEMT, paving the way to opening new high power and temperature applications using solid-state devices, which have normally been held by the vacuum tube technologies.

The microwave transistor is now found in most high-frequency applications in both the military and commercial sectors, and includes mobile communications, satellite links, and radar systems. The FET is used in both very low noise front-end receivers (RX) and high output power RF transmitters (TX), for example, the power amplifier in the base station of the rapidly growing mobile phone business.

1.2 Microwave Device Background

The devices described in section 1.1 are all fabricated using semiconductor materials which include silicon (Si), gallium arsenide (GaAs), indium phosphide (InP) and gallium nitride (GaN) Gallium arsenide and indium phosphide are known as III-V materials due to their position in the periodic table.

A characteristic of all semiconductor materials is that under certain conditions they depart from Ohm's law which is in contrast to metals where, in general, the linear relationship between current and voltage is obeyed.

1.2.1 Energy Bands

Perhaps the easiest way to look at the properties of semiconductor materials is by energy bands. Individual atoms of the crystal are in a periodic structure and are frequently discussed in terms of energy-momentum relationships. For a semiconductor material the energy–momentum (using Schrodingers equation) solution predicts in the energy continuum a forbidden gap which contains no allowed energy levels that electrons can exist. Above and below the forbidden gap energy states can exist and these are known as the conduction and valence energy bands respectively. The energy gap between the highest valence band (E_v) and lowest conduction band (E_c) is known as the energy band-gap (E_g) and is one of the parameters which characterise a particular semiconductor. See Table 1. Gallium Nitride and Silicon Carbide are known as wide band-gap materials because of their very large 'energy band-gaps'.

Table 1 'Band-Gap Energies' of some semiconductors

Semiconductor Material	Room temperature 'Band-Gap Energies'
Silicon (Si)	1.12 eV
Gallium Arsenide (GaAs)	1.424 eV
Indium Phosphide (InP)	1.34 eV
Aluminium Gallium Arsenide AlGaAs	1.773 eV
Silicon Carbide (SiC)	3.6eV
Gallium Nitride (GaN)	3.4eV

For simplicity, most microwave devices only consider the energy band-gap (E_g) and therefore the E-k band diagram can be simplified as shown below in Figure 1.

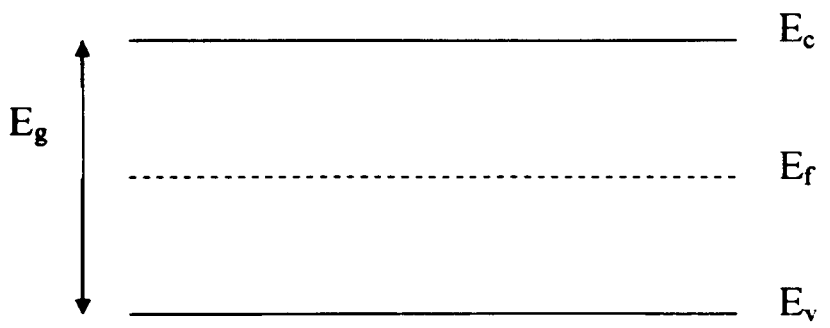


Figure 1 Energy diagram of an un-doped semiconductor material

1.2.2 Semiconductor Doping

To increase the electrical conductivity of the semiconductor a small quantity of an appropriate impurity can be added to the semiconductor this is known as 'doping'. There are two classes of impurity doping which are known as 'donor' (addition of free electrons

in the conduction band) and acceptor (addition of free holes in the valence band) respectively. The introduction of donor atoms into a semiconductor crystal results in 'n-type' semiconductor material, whereas the introduction of acceptor atoms into a semiconductor crystal results in 'p-type' semiconductor material. For silicon typical donor atoms are phosphorus P and antimony Sb, and for gallium arsenide silicon Si and selenium Se.

The band structures for n and p-type semiconductor material are shown in Figures 2 and 3, respectively. The energy levels created by the donors and acceptors are denoted by E_d and E_a respectively.

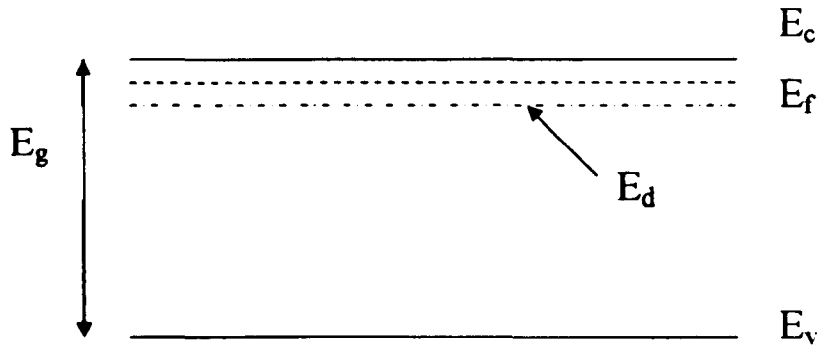


Figure 2 Energy diagram of n-type material

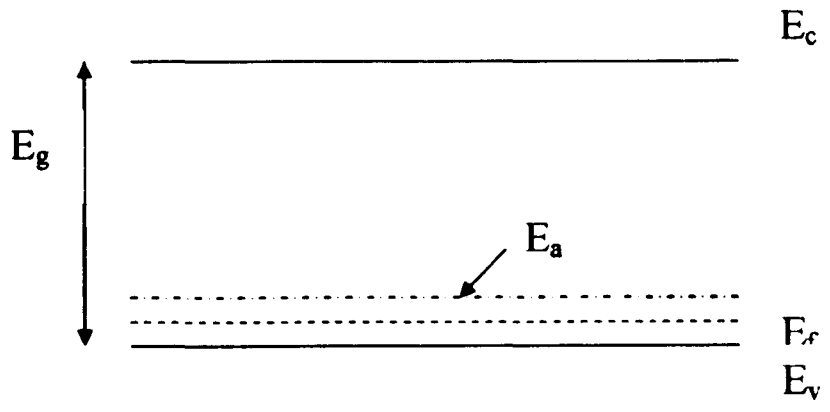


Figure 3 Energy diagram of p-type material

The Fermi level E_f moves close to the conduction band edge for n-type material and close to valence band edge for p-type material.

The relationship for n-type material in terms of the conduction band edge E_c and Fermi level E_f and the available free electrons N_c is expressed as:

$n = N_c e^{(\frac{Ef - Ec)}{kT}}$ N_c is the density of allowable energy states available in the conduction band and varies for a typical semiconductor between 10^{18} to 10^{20} cm^{-3} and kT is the thermal energy of the crystal lattice.

Whereas for a p-type semiconductor the relationship between the valence band-edge and Fermi level and the available free holes is expressed as:

$p = N_v e^{(\frac{Ec - Ef)}{kT}}$ N_v is the density of allowable energy states in the valence band.

In practice, when n or p-type material is required donor or acceptor impurity atoms are chosen that produce shallow energy levels in other words they are in close proximity with the conduction or valence band respectively. At normal working temperatures (room temperature) each impurity atoms produces a carrier, therefore for n – type material $n \approx N_d$ and for p-type material $p \approx N_a$.

1.2.3 Carrier Transport and Conductivity

The electrical current flowing in a semiconductor is determined by the rate of flow of charge and therefore knowledge of both the available charge present and the transport properties are required.

Consider bulk n-type semiconductor material in which a large electric field is applied across it. The electrons are accelerated to velocities greater than the velocity of sound in the crystal. The low-energy acoustic-phonon scattering by which the electrons lose energy to the crystal lattice becomes inefficient hence the electrons gain energy faster than they loose it; therefore the effective temperature of the electrons is greater than the lattice temperature, under these conditions the electrons are called 'hot electrons'. The electrons will now loose energy by the excitation of optical phonons which is a very efficient mechanism for the transfer of energy back to the lattice and results in the average drift velocity of the electrons reaching a limiting value independent of the

magnitude of the applied electric field. Under these conditions the electrons are said to be traveling with a saturated drift velocity, v_s. Therefore, the electric current I through the bulk crystal no-longer increases linearly with the applied voltage, V – it no-longer obeys ohms law.

At even higher electric fields a further mechanism 'impact ionization' becomes very important. In this mechanism the hot electrons suffer collisions with the atoms of the crystal imparting sufficient energy to knock a valence electron free. In terms of the band model, the electron is raised to the conduction band and a hole is left in the valence band. The energy required by an electron to produce an ionizing collision must be greater than the energy band-gap E_g. The electron and hole created by the collision will be accelerated in opposite directions by the high electric field and in turn produce an ionizing collisions producing further electron-hole pairs, therefore a multiplication process. This process is very important in two terminal devices for example the TRAPATT and IMPATT diodes see section 1.2.7). It is also the limiting process in power MESFET and HEMT devices, and hence the interest in wide-band gap materials as they inherently will have a higher gate drain breakdown voltage V_B.

1.2.4 Drift velocity and mobility

The current flow through bulk semiconductor for convenience is often expressed as a current density $J = nqv$, where q is the electronic charge, n the number of carriers and v the average velocity of the electrons or holes. For low electric fields the average electron velocity v is proportional to the electric field E, and therefore $v = \mu_n E$. Where μ_n is the electron low field mobility. Mobility is a material parameter and is a measure of how rapidly an electron or hole can be moved in a semiconductor. Generally, the low field mobility of electrons in materials used for the fabrication of microwave devices is higher than that of the hole; therefore n-type material is generally used for microwave diodes and transistors.

As the electric field is increased, to a first approximation the increased electron velocity will cause the electrons to collide more often and cause the current to decay. A time constant τ_0 proportional to the mean free path can be defined. Hence, a steady-state is

reached when the energy gained from the field exactly balances the energy lost due to the collisions. Therefore:

$\frac{dJ}{dt} = qn\frac{dv}{dt} = \frac{q^2}{m^*}nE$ m^* is the effective mass of the electron or hole

$J = \frac{q^2}{m^*\tau_0}nE$ compare with $J = nqv$

Hence mobility can be written as $\mu = \frac{q < v^2\tau_0 >}{m^* < v^2 >}$ where the velocity dependence of τ_0 is taken into account. The periodic structure of the crystal is also taken into account by the effective mass m^* which departs from the lattice periodicity due to thermal vibrations or ionized impurities acting as scattering centres.

It has been shown, to a first approximation, that at low electric fields the principal scattering mechanisms are acoustic phonon and ionized impurities and that the mobility may be taken as being constant. The semiconductor obeys Ohms law.

At high and increasing applied electric fields the carrier velocity saturates and to explain the saturation effect scattering by optical phonons must be included (section 1.2.3). Optical phonons are high frequency thermal vibrations of the lattice and are not excited at room temperature as $kT << E_{op}$. Where E_{op} is the energy required to excite an optical phonon. When an electron acquires energy greater than E_{op} the probability of the electron loosing the energy by the emission of an optical phonon appreciably increases.

The relaxation time for an optical phonon can be defined as τ_{op} therefore the mobility in the high field region can be written as $\mu = \frac{q\tau_{op}}{m^*}$ in each collision the electron loses energy E_{op}, and so the rate of energy lose can be written as $\frac{dE}{dt} = -\frac{E_{op}}{\tau_{op}}$

The electron gains energy from the field at the rate of $\frac{dE}{dt} = q\mu E^2$ which on average must balance the energy lost in the generation of an optical phonon, hence $\tau_{op} = \frac{(E_{op}m^*)^{0.5}}{qE}$

Therefore, the high electric field mobility is given by $\mu = \frac{1}{E}(\frac{E_{op}}{m^*})^{0.5}$ and is proportional to 1/E, hence the saturation velocity $v_s = (\frac{E_{op}}{m^*})^{0.5}$ is independent of the electric field.

The drift velocity dependence of a number of the more commonly used semiconductor materials in microwave devices as a function of increasing electric field is shown in Figure 4.

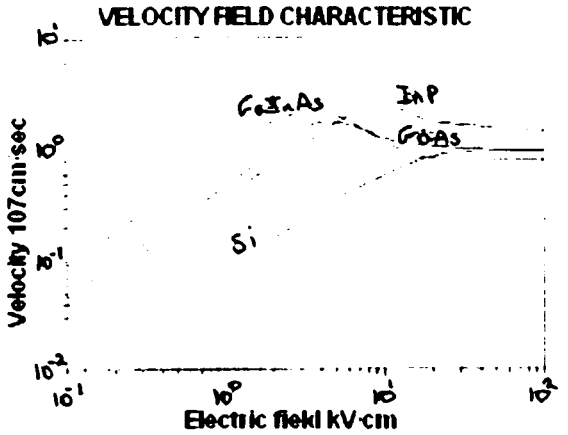


Figure 4 Velocity field characteristics [ref 91]

It can be seen that silicon has a much lower drift velocity in the region where the electric field is around 10 to 20kV/cm and shows no peak in the drift velocity at relative low electric field, unlike GaAs, InP and GaAlAs which all show a distinct peak in the drift velocity before saturation and is a characteristic of the III-V compound semiconductors. The peak in the electric field gives rise to negative differential mobility which results in the Gunn-effect. The Gunn effect is the basis of the operation of the GaAs and InP transfer electron device [3] and is still very important, particularly in the generation of cost effective microwave power at milli-metric frequencies. For this reason the GaAs

Gunn diode is used for the 77GHz TX source in automobile adaptive cruise control systems. The Gunn effect may also affect the operation of MESFET and HEMT devices in what is known as velocity over-shoot.

In addition to an applied electric field across the semiconductor several other mechanisms can act to produce current in a semiconductor structure. These include magnetic fields, radiation and piezoelectric field due to strain being set up in the interface between two different semiconductor materials. The latter is the mechanism used in the high performance wide-band gap GaN HEMT to produce carriers in the 2D electron gas [102].

1.4.2 Impact ionization and avalanche multiplication

In most semiconductors fields in excess of 10^5 V/cm are required before the onset of avalanche multiplication. Once an electron has reached the ionization threshold energy E_i (this is also called the critical field E_c) it is still more likely lose part of its total energy by the emission of an optical phonon and drop below the threshold energy E_i. For an electron with energy E_i the relative probability that the first collision is ionizing is L_{op}/L_i where L_{op} and L_i are the electron mean free paths for optical emission and ionization respectively. The ratio of L_{op}/L_i for an electron at the threshold energy of E_i is between 0.02 and 0.05.

The ionization parameters α and β describe the ionization rates for electrons and holes respectively. The ionization rate is the average number of ionization events by an electron or hole per unit distance traveled in the direction of the electric field. It can be shown [7] that the ionization rate is given by the following expression:

$\alpha = \{\frac{qEL_{op}}{E_{op}L_i}\}\exp\{\frac{E_i}{qL_{op}E}\}$ and it can be seen that α increases rapidly with electric field E.

The above equation can be written in its more normal form as follows $\alpha = A\exp\{-\frac{b}{E}\}^m$ where $A = \{\frac{qEL_{op}}{E_{op}L_i}\}$ and $b = \{\frac{E_i}{qL_{op}}\}$ note that both A and b are temperature dependent. Table 2 gives the room temperature values for A, b and m for Si and GaAs.

Semiconductor	Carrier	A cm^{-1}	B Vcm^{-1}	m	L_{op}	E_{op} eV
Si	e^-	$3.8x10^6$	$1.75x10^6$	1	62	0.063
Si	e^+	$2.25x10^7$	$3.26x10^6$	1	45	
GaAs	e^-	$3.5x10^5$	$6.85x10^5$	2	35	0.035
GaAs	e^+	$3.5x10^5$	$6.85x10^5$	2		

Table 2 parameters giving ionization rates at room temperature for Si and GaAs [7]

1.5.2 Contact Properties

Electrical connection to the bulk semiconductor is extremely important and the connection will often determine the quality of the device. The connections can be ohmic or barrier (p-n junction) depending on the requirement of the device.

1.5.2.1 Ohmic contacts

The electrical properties of an ohmic contact are purely resistive, in other words the applied voltage across the contact is linearly related to the current passing through the contact. Ohmic contacts are critical to the operation of all semiconductor devices. For example contacts made to an IMPATT or TRAPATT diode and the parasitic access source R_s and drain R_d contact resistance associated with a MESFET or HEMT device.

In theory, ohmic contacts [9] are formed by arranging that the work function θ_m of the contact metal is less than the work function θ_s of the a joining semiconductor. The Fermi levels are aligned by the transfer of electrons from the metal to the semiconductor, thereby raising the semiconductor electron energies enabling under bias the flow of electrons across the barrier with minimal resistance.

Often in practice a high density of surface states exist on the surface of the semiconductor, and in band theory terms, exist within the band gap pinning the Fermi level regardless of the metal work function. Therefore real ohmic contacts are fabricated by very heavily doping the contact semiconductor which results in a very thin (tens of angstroms) surface depletion layer in which the electrons can tunnel through the barrier rather than having to climb it.

Many receipts for good ohmic contacts appear in the literature and processes were developed for the devices [A1, A3, B2, and B4] presented in this thesis.

1.5.2.2. The p-n junction

A further very important contact is the rectifying contact which provides the switching mechanism particularly in transistors. The rectifying contact can be a p-n junction or a Schottky junction where the metal semiconductor provides the rectification.

The basic p-n junction is shown in Figure 5.

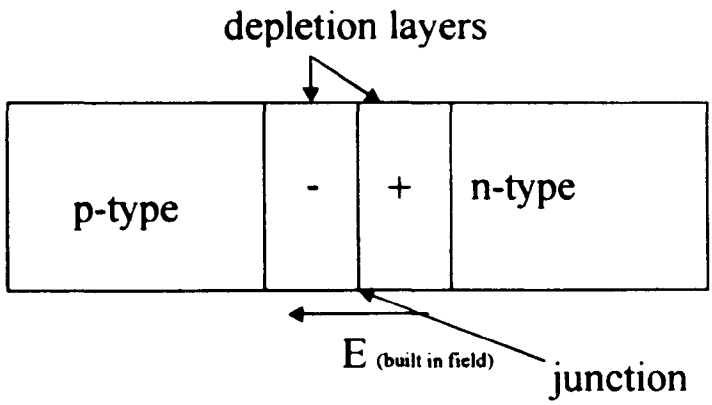


Figure 5 p-n junction

The p and n-type material are brought together e^+ diffuse into the n-type material and e^- diffuse into the p-type material resulting in a space charge region around the junction and the resulting built-in electric field opposes further diffusion I_{diff} of the e^+ and e^-. The drift current $I_{thermal}$ to the thermal generation of electron-hole pairs diffuse across the space charge region and are subsequently swept down the potential barrier by the built-in electric field. With no bias applied across the pn junction the external current I flowing in the circuit is zero [9].

$$I = I_{diff} - |I_{thermal}| = 0$$

When a battery is connected across the pn junction in such a way that the p-type material is connected to the +ve terminal and the n-type material is connected to the –ve terminal, the pn junction is said to be forward biased. The electrostatic potential of the p side is raised in comparison with the n side, hence lowering the potential barrier, enabling the e^- and e^+ respectively, to diffuse across the junction. The diffusion current I_{diff} across the junction therefore increases. The diffusion current is increased by a factor $e^{\frac{qVf}{kT}}$ over its equilibrium value I_{diff} where Vf is the applied forward bias. In equilibrium $I_{diff} = I_{thermal}$, therefore in forward bias condition $I = I_{thermal}[e^{\frac{qVf}{kT}} - 1]$ which is the well known pn junction or diode equation.

Under reverse condition, the electrostatic potential of the p-side is further lowered with respect to the n side thereby increasing the barrier height, hence there is virtually no diffusion of the majority carriers. The diffusion current is in fact reduced by the factor $e^{\frac{-qVr}{kT}}$ over the equilibrium I_{diff}.

To take account of recombination in the space charge region the diode equation is corrected by including a factor n known as the ideality factor, therefore the diode equation becomes:

$$I = I_{thermal}[e^{\frac{qV}{nkT}} - 1]$$

The reverse bias across the diode can be continually increased until avalanche breakdown occurs (see section 1.4.2) and is the principle of TRAPATT and IMPATT diodes (see section 1.2.7) and the limiting factor of power transistors (Chapter 5).

In the forward direction most diodes will deviate from the above diode equation at high current levels, this is primarily due to ohmic losses in the metal contacts and resistive losses in the neutral regions of the p and n materials. These losses are often accounted for by a single series resistance in an equivalent circuit of the diode. Later discussion in the thesis will cover the importance of these parasitic diode resistances with reference to the MESFET and HEMT transistors.

1.5.2.3 Capacitive nature of pn junctions

Two types of capacitance are associated within the pn junction. These are the junction capacitance C_{jun} and the diffusion capacitance C_{diff}. The junction capacitance is due to the space charge at the junction interface and therefore will dominate under reverse bias conditions. The diffusion capacitance dominates in the forward bias condition and is due to the majority carrier diffusing across the junction and becoming a minority carrier (for example e^- diffusing from n-type to the p-type). The minority carrier (for example the e^- in the p material) will then recombine with a e^+. The recombination process has associated with it a characteristic time τ_e for electrons and τ_p for holes. The stored charge is then $Q_n = I_p\tau_n$ and $Q_p = I_n\tau_p$ where I_n and I_p are the diffusion currents due to the injection of e^- into p-type material and the injection of e^+ into the n-type material respectively [9].

The microwave devices being considered in this thesis will be reverse biased. The gate to source junction of a FET is a reverse biased pn junction and therefore the dominant capacitance associated with that junction is the junction capacitance C_{jun}.

1.5.2.4 Schottky Barrier Junction

The Schottky junction consists of a thin metal layer deposited on a semiconductor. The work function ϕ_s of n-type semiconductor is normally greater than the work function of

the metal ϕ_m (see section 1.2.5.1) this will result in electrons from the semiconductor transferring to the surface of the metal. This charge resides on an infinitesimally thin layer while the width of the induced positive charge in the semiconductor will be a function of the doping density. Hence, the higher the doping density of the semiconductor, the smaller the width of positive charge will be required to balance negative charge on the metal. The behavior of the junction is therefore very similar to that of a pn junction and the diode equation $I = I_{thermal}[e^{\frac{qV}{nkT}} - 1]$ is directly applicable.

As no minority carriers are involved in a Schottky diode, there is no diffusion capacitance associated in the forward bias condition, hence its switching speed is greater than that of a pn junction. For this reason Schottky diodes are normally used as the gate to source junction device for microwave FET and HEMT transistors.

1.6.1 MESFET devices

A short description of the MESFET will be given as a preview to a more complete description given in Chapter 3 of this thesis.

A cross section of a simple single cell n-type MESFET is given in Figure 6.

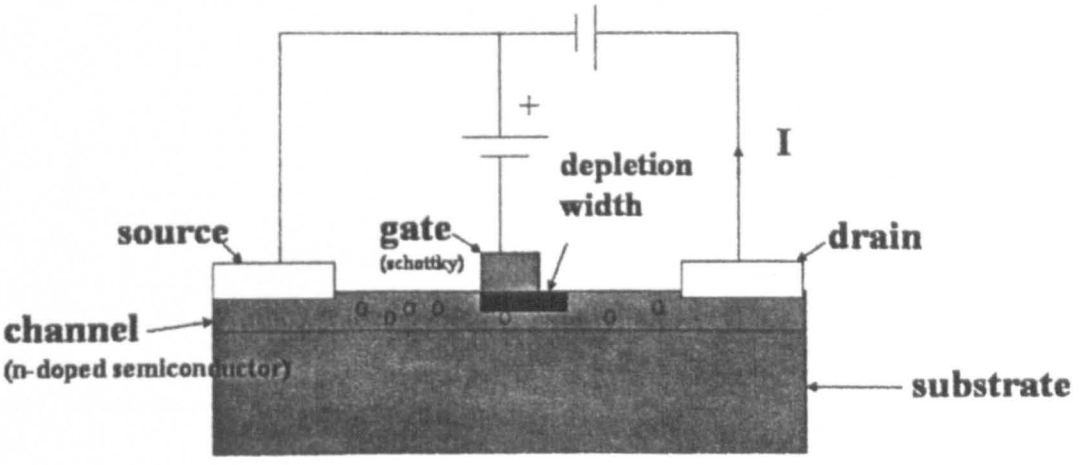


Figure 6 MESFET

It consists of two ohmic contacts, the source and drain, to which an electric potential is applied across them (see Figure F), the drain being positive with respect to the source.

The resulting electric field accelerates the carriers in the channel region and provided the electric field is sufficiently large the carriers will reach their saturated velocity (v_s), under the gate. Geometrically between the source and drain contacts is the metal Schottky gate contact, which is biased negative with respect to the source (reverse biased).

For microwave and millimetric devices the channel region is normally n-type gallium arsenide. This layer can be fabricated for example by vapour phase epitaxy (VPE), ion implantation, molecular beam epitaxy (MBE) or metal organic vapour deposition (MOCVD) for a more complete description of these processes see reference [26]. The active doping of the channel region will determine the thickness of the active region and there appears to be an optimum ratio for a low noise MESFET which is discussed in further detail in chapter 3.

A plan view of the MESFET is shown in Figure 7

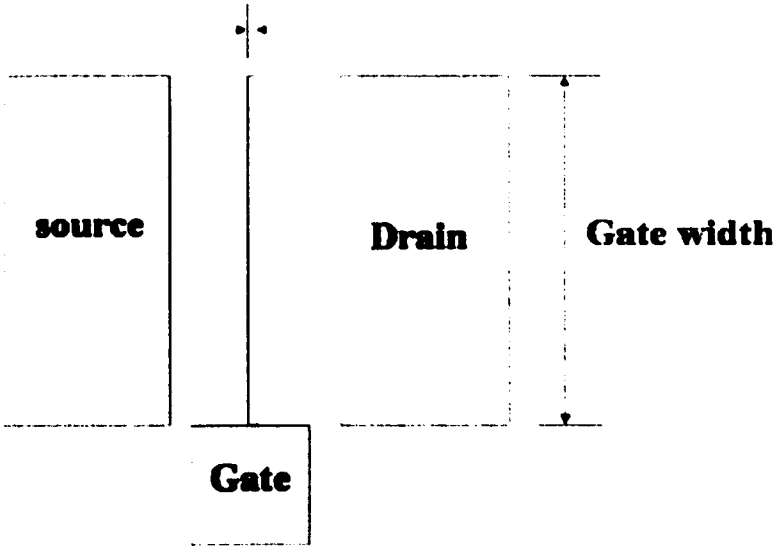


Figure 7 Plan view of a single cell MESFET

The gate length (Lg) determines the frequency of operation of the device and for RF and microwave devices can be between 2 and 0.1 micron. Gate dimensions below 0.5 micron are normally realized by electron beam (EB) lithography [B4]. Another important

geometrical dimension is the gate-width (W) of the transistor and will determine the current capability of the device. For example, a low noise small-signal MESFET will have a small gate-width, typically < 0.2mm for a 10GHz transistor, whereas a power transistor will have a very wide-gate width, many mm. The spacing (Figure G) between the source and gate finger is known as the gate-to-source (L_{gs}) spacing, and the spacing between the drain and gate finger is known as the gate-to-drain (L_{gd}) spacing. Both play an important role in the operation of the transistor in that they help to determine the magnitude of the parasitic source and drain resistances respectively. The gate resistance (R_g) is the ohmic resistance of the gate strip and will significantly increase as the gate-length is decreased. 'T' profile gate structures are used to reduce the gate resistance and which is fully described in Chapter 4 on travelling wave structures.

To extend the total gate width of the MESFET multiple single cell structures (Figure 8) are used. If a single very wide gate width was used, the input signal travelling down the gate would be attenuated and therefore at the far end the structure the input signal would no-longer modulate the channel current, in simple terms there would be no gate action. To overcome this problem multiple single cell structures with short gate widths are paralleled together to provide the total gate width.

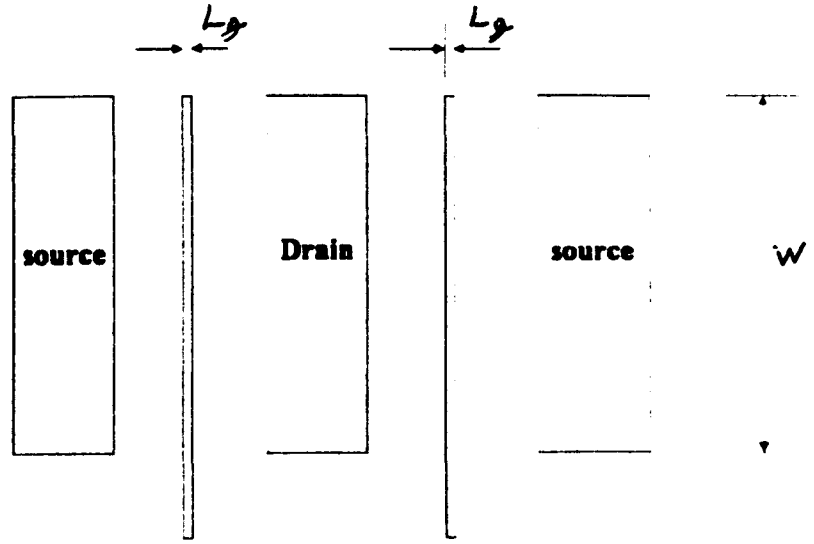


Figure 8 Multiple cell MESFET

1.6.2 High Electron Mobility Transistor (HEMT)

The high electron mobility transistor is a hetero-junction device offering improved performance over the MESFET. The device has a high electron mobility and velocity as the carrier electrons are restricted to a potential well in un-doped material, thereby minimizing ionization scattering.

Figure 9 shows a simple schematic of the cross-section of a single cell HEMT device.

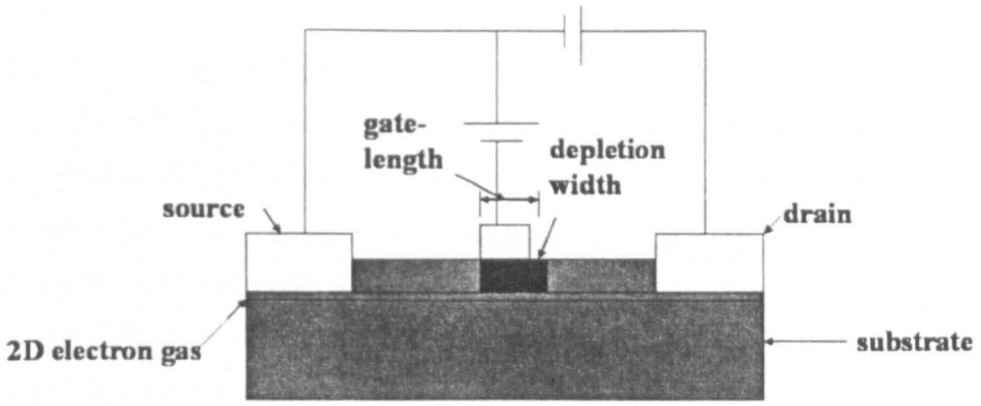


Figure 9 schematic of a HEMT

The geometry and terminology is identical to the MESFET, and again the source and drain contacts are ohmic and the gate is a Schottky barrier contact. Further similarities diminish rapidly as the operation is distinctly different.

The fabrication of the device is more complex as it relies on a semiconductor interface between wide and narrow band-gap semiconductors. The most common used are aluminum gallium arsenide (AlGaAs) and undoped gallium arsenide (GaAs). The thickness and doping density of the AlGaAs layer is designed so that under normal operating conditions the layer is completely depleted of electrons. The undoped GaAs layer has to be of very high quality (no defects). Other material combinations can be used to good effect for example aluminum gallium nitride (AlGaN) and un-doped gallium nitride (GaN) these devices are covered in detail in chapter 6.

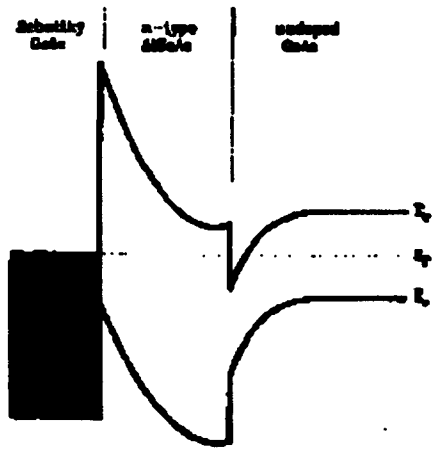


Figure 10 band diagram of a simple HEMT (AlGaAs/GaAs) [9]

Figure 10 shows a Schottky diode fabricated on the AlGaAs (n-type wide band-gap material) which is depleted of free carriers by the reverse or zero-biased Schottky contact. The un-doped GaAs on the right is the narrow band-gap material. At the boundary between the two materials there is a discontinuity in the conduction band which causes it to dip (often referred to as a potential well) below the Fermi level. At this point (section 1.2.2) there is a very high concentration of free electrons essentially in the un-doped GaAs. Note, the region of high concentration of electrons is extremely thin and is therefore often referred to as a sheet concentration (n_s) or 2D electron gas sheet. Electrons travelling in the 2D gas layer are not impeded by ionized donor atoms and therefore approach high mobility and saturation velocity. By increasing the negative bias on the metal Schottky contact will raise the conduction band layer of the AlGaAs thereby reducing the depth (in electron energy) of the potential well, so causing a reduction in the sheet concentration of free electrons in the un-doped GaAs.

Contact with the 2 D gas layer is made by fabricating very heavily doped, low resistance source and drain wells. At low values of drain source bias voltage an electron current flows from source to drain within the 2D gas layer. When a voltage is applied to the gate the sheet concentration of the 2D gas layer is modulated. For a sufficiently large negative voltage applied to the gate, the 2D sheet concentration becomes very small, and the device is said to be pinched-off.

The current voltage characteristics of a HEMT are very similar to those of a MESFET. The transconductance (g_m) is defined as the slope of the I_{ds}- V_{gs} transfer characteristic

with the drain source voltage V_{ds} held constant. The parameter is used to indicate the performance of both MESFET and HEMT devices. Normally device, with identical gate-width, which provides the highest transconductance will give superior gain, noise and high frequency characteristics, this will be discussed in detail in chapters 3, 4 and 5.

1.2.9 Reverse bias pn junctions - the TRAPATT and IMPATT diodes

In sections 1.5.2.2 the pn junction was covered including reverse biasing the diode to its reverse breakdown voltage (V_B). The reverse biasing of pn junctions leads to a number of interesting microwave types of device. Two of these devices will be briefly described as they are efficient microwave generators and can also be used in reflection type of amplifiers. These devices are known as the Impact Avalanche Transit Time (IMPATT) and Trapped Plasma Avalanche Triggered Transit (TRAPATT) diodes. The IMPATT is still of great interest to the microwave community for the generation of milli-metric waves (70 to > 500GHz) while the TRAPATT has found a niche in low microwave frequencies (1 to 2GHz) as a high power short pulse generator.

The negative resistance in an avalanche device occurs as a result of 180^0 phase difference between the external circuit ac current and voltage when a p-n junction is reverse-biased into avalanche breakdown. The phase difference is produced by the time delay inherent in the build-up of the avalanche (AVALANCHE DELAY) current, coupled with phase delay developed as the carriers traverse (TRANSIT TIME DELAY) the depletion layer. The origin of the phase delay in both the above processes will be considered in a simplified model of the IMPATT diode.

First consider a very simple IMPATT diode shown in Figure 11 and which is reverse biased.

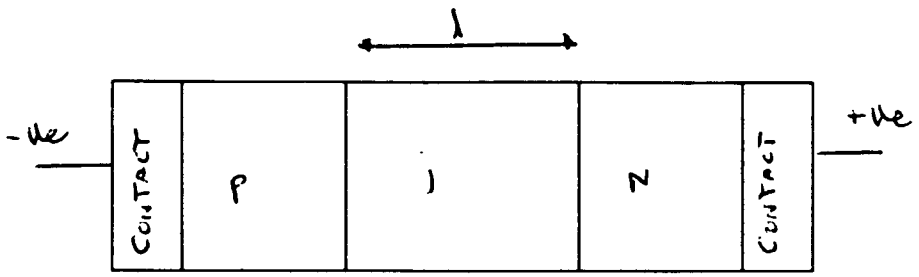


Figure 11 p-i-n IMPATT diode

Assume that the intrinsic region is of length l completely depleted of e^- and a high electric field $>E_s$ exists across this region which is greater than required to produce saturation of the electron drift velocity. If at time $t = t_1$ an e^- bunch is injected into the high-field region, the e^- will drift across the sample to the +ve terminal and will be collected at the cathode at a time $t = t_1 + \tau$, where τ is the transit time. When e^- are injected into the high-field region, charges are induced on both cathode and anode electrodes and a current starts flowing in the external circuit. As the e^- drift across the transit region under the influence of the high electric field, the induced charge on the electrodes vary and so the current continues to flow until the e^- reach the anode when the induced current will disappear. Therefore, the current starts instantaneously, when charged is injected, but still flows τ seconds later. Hence on average the current flowing in the external circuit is delayed by $\tau/2$ relative to current injected at the cathode.

If a sinusoidal time-varying current field is superimposed on the steady field in such a way that the amplitude is small enough for the e^- to remain at the saturation velocity and by delaying the carrier injection by one half cycle the condition for power generation is obtained, see CASE III in figure 12. The transit time on average provides 90^0 of phase shift and further 90^0 of phase shift is provided by injection of the e^- into the transit region.

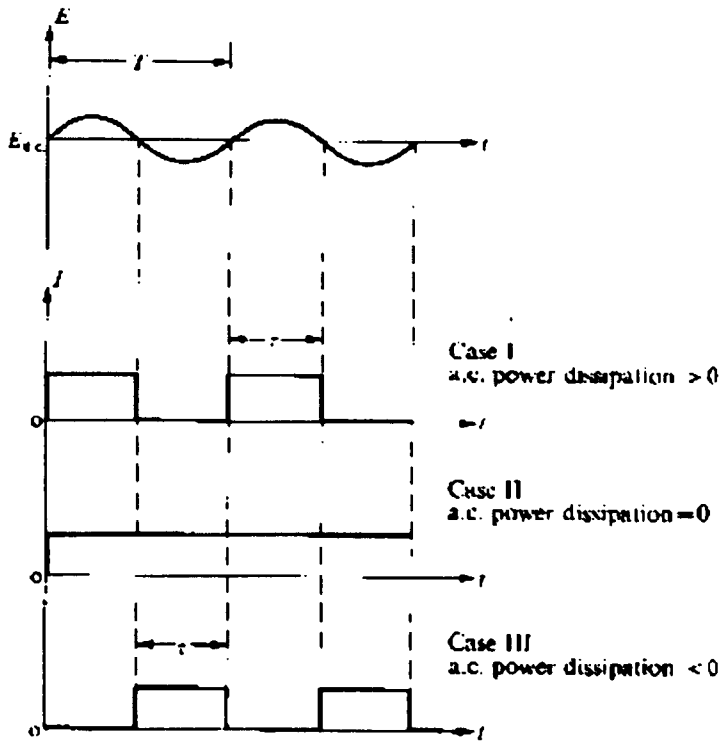


Figure 12 CASE III 180° phase delay, ac power generation

When a p-n junction is reverse biased into avalanche breakdown (see section 1.2.5) the current builds up from impact ionization which takes a finite time after the application of the voltage. If a diode is dc biased to the breakdown voltage V_B and a sinusoidal time-varying voltage is superimposed on the dc voltage then during the +ve half of the cycle the diode will go into avalanche and the current will build-up, whereas during the –ve half of the cycle the voltage is below the breakdown voltage and the current will decay, see Figure 13.

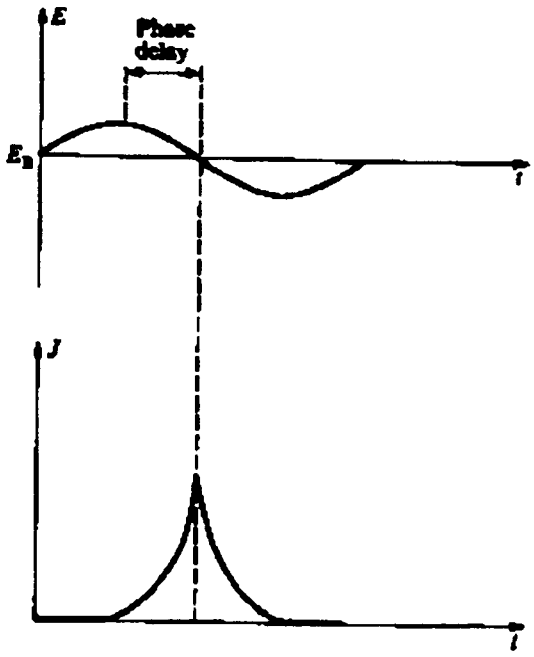


Figure 13 90° phase delay due to Avalanche delay

Thus the avalanche current will peak 90^0 after the voltage has peaked (AVALANCHE DELAY), this delayed current pulse is then injected into the drift zone where it experiences a further 90^0 phase delay (TRANSIT-TIME DELAY).

By selecting the correct transit time and coupling the diode into a electrical resonant circuit, high frequency oscillators can be realised. The transit time which will be dependent on the semiconductor and the thickness of the low doped (intrinsic) transit region will determine the frequency band of operation. The IMPATT diode is still one of the most powerful solid state sources of microwave power particularly in the milli-metric frequency band (> 30GHz) which is only now being challenged by the wide band-gap compound semiconductor HEMT devices (see chapter 5). However, there are two inherent difficulties with the IMPATT diode technology these are (1) high noise and sensitive to operating conditions and (2) large output electronic reactance which are strongly dependent on oscillation amplitude and require very careful circuit design. These inherent problems will eventually move the IMPATT diode into niche applications with the further maturity of the microwave transistor.

A further IMPATT related device is the TRAPATT diode. The TRAPATT mode of operation was discovered by Prager, Chang and Weibrod in 1967 [9] when using silicon

avalanche diodes. The operating frequency is considerably lower than the IMPATT transit time and the dc to RF efficiency very much greater than can be obtained from the IMPATT diode. Theoretical work has shown that the diode goes into avalanche at the high-field side and sweeps rapidly across the diode, filling it with plasma of e^- and e^+ whose space charge depresses the voltage to a very low level, thereby trapping the plasma, hence the name trapped plasma avalanche triggered transit (TRAPATT) diode. The microwave operation of the TRAPATT diode is fully described in section 2.5 of chapter 2. The diode initially appeared to exhibit properties which would make it useful for high-powered radar applications up to X-band frequencies (8.4 to 12.4 GHz), this area is fully dealt with in chapter 2 and represents the first major research carried out and published by the author.

1.3) Rational for Studying the Solid State Devices in this Thesis

In the mid 1970's many industrial research areas were heavily involved in the development of solid-state devices for low noise front-ends and high-power amplifiers for high-frequency applications. The TRAPATT diode had been identified as a possible contender from early work published by Bell Labs (USA). The TRAPATT mode offered a very high efficiency and high pulsed RF power suitable for oscillators and reflection type of amplifiers and could be powered using relatively low voltages when compared with the valve technologies. The work at Plessey Research, Caswell, was funded by CVD to develop a high power silicon TRAPATT diode primarily suitable for X-band (8.4 to 12.4GHz) airborne applications. The development of the device was very successful and preliminary work indicated the feasibility of running the device as a reflection amplifier in a class C mode enabling the possibility of very high amplifier efficiencies, a requirement in airborne applications. Also, the amplifier could be run directly from a low dc voltage rail (25V) without having to include high voltage converters as required for valve power amplifiers. It was also perceived that solid state devices would offer high reliability and greater packing density. The published work highlighted in this thesis describes the optimization of the TRAPATT diode to operate over relatively long pulse widths (5 microseconds) and high duty factors (10%) as required for pulsed airborne radar. A major part of the work was the development of the reflection amplifier circuits

and in particular cascading gain stages together to obtain high gain and RF output power, as well as maintaining the efficiency and providing a rugged solution. This work was seen as pioneering at the time.

Towards the close of the development it was clear that matching the device particularly at X-band fundamental frequencies was extremely difficult, as the higher order harmonics also had to be matched for both clean switch-on and pulse operation. Some of this problem was attributed to rapid frequency change (chirp) across a pulse due to the rise in temperature; this was still found to be a problem even after very high levels of thermal management were designed into the diode. The penultimate of the work was the design and demonstration of a 3 stage power amplifier. The overall efficiency was much less than predicted due to the significant amount of electronics required to compensate for the chirping and to provide protection to the diodes.

Although the development was very rapid, other devices were advancing very quickly, in particular the MESFET, which was perceived as the way forward in the longer term primarily because of easier circuit solutions. The TRAPATT work concluded that the device would offer a solution to applications at low frequencies L-band (1 to 2 GHz) where circuit solutions were much easier as the fourth or fifth harmonics were still below10GHz. Interestingly, the TRAPATT diode at a later date found an application as a proximity device working in L-band.

At this stage the author became involved in the rapid MESFET development and in particular the quest for high-frequency and low noise, which were required for satellite and communication links. Plessey, Caswell was well positioned to develop the GaAs MESFET which was built on the pioneering work of Jim Turner OBE.

The author was primarily involved with the development of a low parasitic GaAs MESFET device with a 0dB cut-off frequency well in excess of 50GHz which became known as the C1 device. The transistor utilized a 0.25 micron gate-length which was drawn by electron beam lithography. This technology had originally been developed by R. Bennett at Caswell for direct writing the multi-finger acoustic surface wave transducers. The author developed circuit measurement and analysis techniques to enable the device characterization to 40GHz. The characterization included minimum noise figure (NF_{min}) measurements of 3.2 dB at 32GHz which were some of the lowest report

in the open literature in the early to mid 1980's. The work led to the hypothesis that at high frequencies the transistor electrodes should be considered as transmission lines. The work naturally complimented the theoretical predictions of a growing wave in a travelling wave transistor (TWF) which were being developed by D.Rees (RSRE Malvern). The concept of a growing-wave would enable the gain to increase with the geometrical length of the TWF.

The author subsequently became involved in developing the TWF in-line with the work of D. Rees. This era was particularly exciting with the realization of a travelling wave structure using overlay capacitors in the drain circuit to balance the velocity of the waves on both the gate and drain electrodes. The transistor was fed by 180^0 balun circuit splitting the input signal equally between the gate and drain electrodes, a similar circuit was used at the output of the transistor i.e. the other end of the active transmission line. To the authors best knowledge this was the first experimental evidence of a growing wave in a travelling wave transistor. The work led to showing that there were a number of disadvantages with the TWF the prime one being the device was reciprocal $S_{21} = S_{12}$. The quest to obtain a practical TWF structure was funded by MOD and INTELSAT. A new structure was developed which became known as the linear gate transistor (LGT) and was subject of an international patent. The transistor was non-reciprocal $S_{21} \# S_{12}$ and evidence of a growing-wave was theoretically and experimentally verified. Work on this device was curtailed in the late 1980's for two reasons (a) the technology to fabricate a LGT giving significant advantages over the travelling wave amplifier TWA was not available and (b) the down turn in defence spending along with the demise of Plessey Company. This period brought many exciting and innovation programmes to a premature close with the inevitable decline in the UK position in many areas of electronic engineering.

During the late 1990 the author became involved with the development of microwave and RF transistors fabricated on wide band-gap materials, for example gallium nitride (GaN). Many of the technologies, characterization methods/models developed for the gallium arsenide devices in principle could be adapted to devices being fabricated on the wide band-gap materials. This was particularly seen with the use of the simple Fukui noise model to predict to a first order of magnitude the minimum noise figure of the AlGaN

HEMT, and to the authors' best knowledge represented the first openly published noise model for a GaN transistor. This work has now been extensively extended to include the effects of gate leakage and cross-coupling between the gate and drain electrodes.

CHAPTER 2: HIGH POWER MICROWAVE AMPLIFIER for I-BAND

2.1) Introduction

In the early 1970's there was a requirement for a high efficiency X-band power amplifier technology, which would run off a low voltage source, primarily for an airborne application. The GaAs MESFET was not a sufficiently mature technology at the time, and there was a world–wide interest in the RF capability of the recently discovered high efficiency TRAPATT (trapped avalanche plasma trigger transit) mode in providing a well behaved microwave high-power source in X and J-band for both oscillator and power amplifier components.

The potential of obtaining high microwave power from the device in a stable and well behaved reflection power amplifier, which would run from a low voltage supply, was an attractive alternative to the high voltage vacuum tube.

2.2) Reflection amplifier

A single-stage reflection amplifier using a circulator is shown in Figure 14.

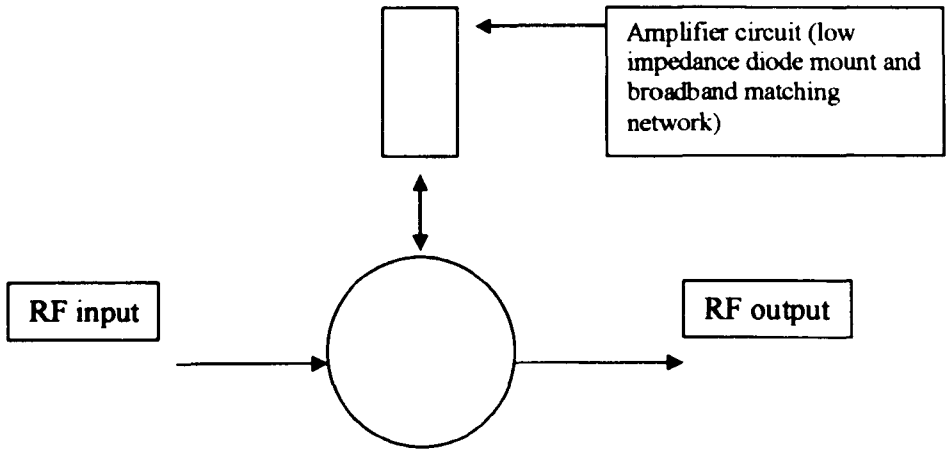


Figure 14

Single-stage reflection amplifier

The reflection amplifier [17, 18] separates the input from the output signal using a circulator. A negative resistance device is used as the active component in the amplifier circuit **[I4].**

There are 4 design requirements:

a) The microwave package should be transparent at the frequency of operation.

b) A broadband and low impedance matching-network is required at the device terminals to present the correct impedance to the diode over the bandwidth.

c) A broadband matching network is required to transform the circuit impedance to the circulator impedance.

d) The circulator should offer a-well-behaved impedance over the required bandwidth.

2.3) The TRAPATT mode

The TRAPATT mode in a heavily punched [19] through diode, was discovered in 1967 by Prager, Chang and Weisbrod [9]. It was characterised by very high dc to RF conversion efficiencies, with a sudden decrease in voltage across the diode, and consequently a rapid increase in current at the onset of oscillation. Several authors, including the research work carried out by the author **[A5],** reported efficiencies in excess of 35% in I-band (8.4 to 12.4 GHz) and measured RF pulse output powers of up to 15watts, at 8GHz. The work carried out by author **[A5],** also showed that output powers and efficiencies of 3.5 watts and 13 % respectively, were experimentally feasible by extracting the second harmonic at 18GHz and probably represent one of the highest recorded measured RF performance from a J-band TRAPATT oscillator **[I1].** The reported high-conversion efficiencies of the TRAPATT diode in an oscillator or amplifier mode **[A5]** made it a possible contender for the solid-state replacement of medium pulsed power travelling wave tube (TWT) amplifiers at frequencies approaching 10GHz. The published work describes the TRAPATT diode, circuit design details, the realisation and characterisation of a three-stage TRAPATT amplifier operating at a centre frequency of 9.7 GHz **[A1].** The amplifier operated in a class-C mode, only dissipating power during the input signal duration, thereby potentially providing a high efficiency of operation

from a single-shot pulse, to a high-duty factor. The research work was conducted over approximately four years.

2.4) Target Specification for I-band TRAPATT Amplifier

A target specification for the amplifier was given at the onset of the research project to investigate the feasibility of a solid-state power-amplifier for application in air and ship-borne radar systems. The research included environmental conditions, for example, vibration and temperature performance. The project was funded by the Ministry of Defense, (MOD), along with private venture money from Plessey Co Ltd. At the time of the research project, high RF peak power capability at high duty-factors and long pulse-widths were provided by the high-voltage vacuum tube technologies.

Research Target Specification

a) Centre frequency 9.7GH$_z$

b) Bandwidth 100MH$_z$

c) Peak power 15Watts

d) Efficiency 10%

e) Pulse width 0.25 to 3.0 microseconds

f) PRF single shot to 33 kH$_z$

g) Supply voltage 40 +/- 1V

h) Temperature –10 t0 60^{0}C

The amplifier design required research in all aspects, including diode design, amplifier circuits and cascading of the TRAPATT circuits, which had not been reported in the literature by other research organisations. The research project led to the first I-band multi-stage class C amplifier reported in the literature **[A1]**.

2.5 TRAPATT Device Operation, Design and Fabrication

2.5.1 Operation

The TRAPATT diode consists of a p^+nn^+ profile, see Figure 15. The n region is made very narrow so that when a reverse voltage is applied the n-region is fully depleted of carriers before the diode reaches its static breakdown voltage. Therefore, when a very rapidly increasing reverse voltage which is greater than the static breakdown voltage is applied across the device an avalanche zone will propagate through the depletion layer resulting in a hole and electron plasma, switching the diode into low voltage and high current state. The electric field in the device thus approaches zero and the drift velocity of both the electrons and holes drop well below the saturated value, and the carriers are said to be 'trapped'. The carriers now slowly drift out of the active region Figure 15 (e^- to the right and e^+ to the left) with velocities well below saturation, thereby the electric field slow recovers and the voltage across the diode increases. The slow process of the carriers drifting out of the active region dominates the transit time and thus the frequency of operation of the device, therefore the oscillation period is very much greater than for an IMPATT diode. The voltage is said to be fully recovered when the last carriers have drifted out of the active region and the current has returned to a low value. The process then repeats itself so the diode cycles between high voltage, low current and low voltage high current states. The voltage and current waveforms are favourable in obtaining very high DC to RF conversion efficiencies.

To operate the TRAPATT mode the diode is placed at the end of a coaxial cable cavity and the bias supplied via the inner conductor of the coaxial line. Tuning slugs are then used to match the diode at the fundamental frequency for optimum power transfer to the load. The first tuning slug is always $\lambda/2$ distance from the diode, where λ is the wavelength of the fundamental mode.

The operation of the TRAPATT as an oscillator can now be described. It is believed [7] as the voltage applied to the TRAPPATT diode is increased IMPATT oscillations are initiated locally to the diode. These oscillations provide the required rapid voltage impulse above the static diode breakdown resulting in the trapped plasma mode and in the voltage across the diode collapsing. The resultant negative voltage pulse then propagates down the transmission line, where it is reflected at the first low impedance

matching section resulting in the voltage pulse being propagated back to the diode as a positive going pulse. This reflected pulse will provide the positive going pulse to trigger the next TRAPATT cycle. It is clearly seen that the distance between the diode and the first low impedance matching section is required to be $\lambda/2$, in order to maintain the triggering for the fundamental mode of the TRAPATT oscillator.

2.5.2 Design and Fabrication

The TRAPATT diode design required special consideration, in order to operate reliably at the high current densities, and to dissipate the high levels of dc energy. To minimise the voltage drop across the resistive contacts and parasitic losses between the diode and circuit interfaces, the following were carefully investigated during the research programme:

a) The impurity doping profile of the material to enable reliable operation at high current densities.
b) Novel thermal management design of the diode to dissipate high levels of pulsed dc energy.
c) Low electrical contact resistance and electrical parasitics between the diode and package to minimise dc losses and device circuit interaction.

The impurity doping profile of a conventional p^+nn^+ TRAPATT diode consists of a narrow n-type active region with abrupt p^+n and nn^+ interfaces. A very high degree of control of the n-region doping level and thickness is required **[A1].** As the reverse voltage across the diode is increased the depletion layer moves through the n-region, and provided the n-region is sufficiently narrow, will reach the n^+ region before the p^+n junction reaches the avalanche breakdown voltage (Figure 15).

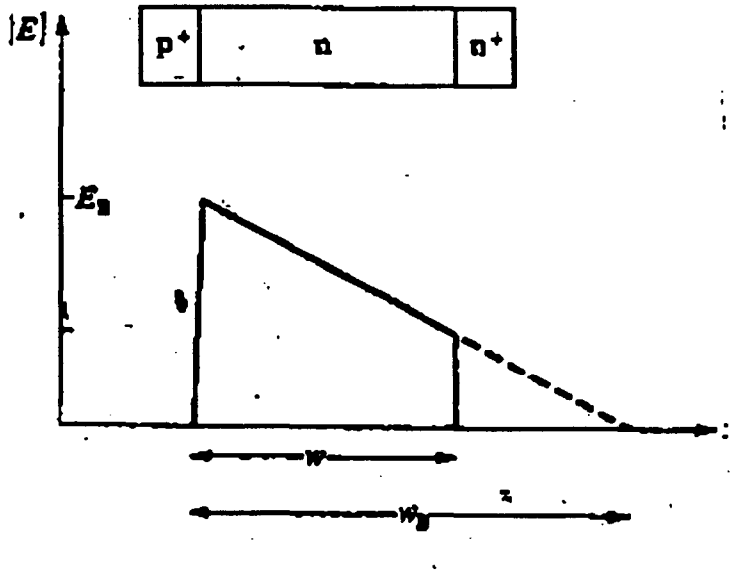


Figure 15: Diode punch-through

The punch-through factor (F) is defined as $F = [V_B/V_P]^{0.5}$. Where V_B is the breakdown voltage of the p^+n junction of a non-punch through diode with the same doping density as a punch-through diode, and V_P is the punch-through voltage. The punch-through factor was experimentally optimised and found to be the order of 6 **[A1, A4 and A5]**, similar to other reported work [16].

The experimental work **[A5]** showed that an abrupt p^+n junction was prone to premature burn-out, whereas a graded p^+n junction was found to more readily withstand much higher current densities, commensurate with high RF conversion efficiency. The n^+n interface was designed to be abrupt to minimise parasitic resistive loss under large signal operation. The doping profile used is shown in Figure 1, page 464 of **[A1]**, and it was experimentally found that for optimum I-band operation the diode breakdown voltage required to be between 28 and 34 volts. A full description of the material requirements and diode fabrication is given on pages 464 to 465 in **[A1]**.

2.6 Thermal Design

To obtain the very high peak power from the diode it was necessary to efficiently remove the Joule heating being generated at the diode junction. A novel approach was adopted to minimise the pulse thermal impedance (θ_{pulsed}) of the diode. It consisted of a gold integral

heat sink (IHS) on the front contact of the diode and a gold-plated heat reservoir on the back contact of the diode, thus enabling heat to be extracted from both sides of the junction during the pulse duration **[I1,I2,I3].** A schematic of the diode is given in Figure 2, page 465 **[A1].** The gold reservoir was required to have sufficient mass for its temperature not to change appreciably during the duration of the pulse and the time taken for the heat to reach the reservoir was required to be less than the pulse-length.

A simple 1-D thermal model was developed by J. Purcell to investigate the thermal requirements of the diode and is given as back-ground information. With reference to Figure 16, consider a step in temperature of T_0, due to heat being generated at the junction of the diode. The heat will flow out of the junction in both directions. The temperature change can be approximated to the equation describing the charging of a capacitor via a resistor.

$$T = T_0(1 - e^{-t/RC}) \qquad (2.5.1)$$

Where R = thermal resistance of the semiconductor

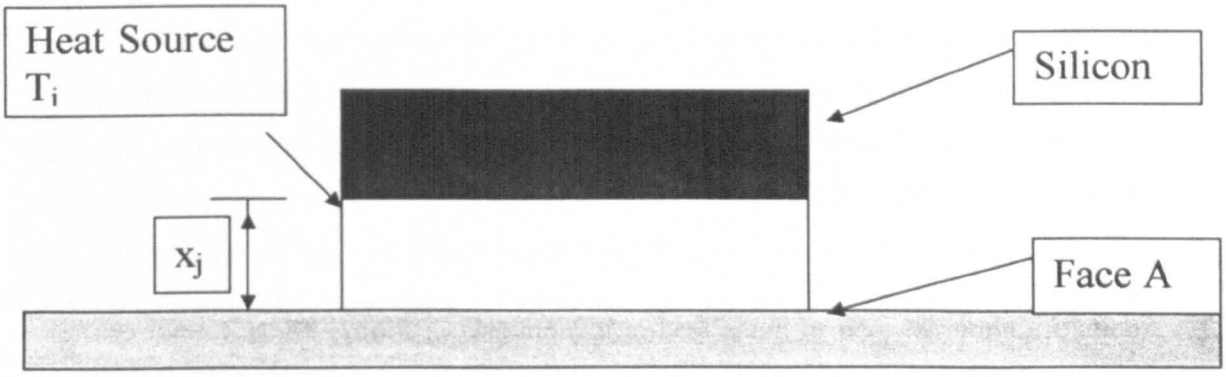


Figure 16 Simple 1D thermal model

C = heat capacity of the heat-sink

T = temperature after time t

t = time in seconds

$R = x/(kA)$

$C = C_p \rho A$

x = thickness of the semiconductor

A = cross-section area

ρ = density

C_p = specific heat

k = thermal conductivity

α = diffusivity (0.495 $cm^2.sec^{-1}$ for silicon)

Further, consider Figure 16, the time taken for the face 'A' to reach 0.9x temperature of the junction (T_j) is given by:

$$t = (x^2/\alpha) \ln(10) \text{ seconds} \qquad (2.5.2)$$

The equation shows that for a pulse width greater than 500nS the contribution to the thermal impedance of the device, by a 3 microns thick layer of silicon can be considered as a constant and equal to the steady-state value.

To extract heat from the back of the diode, a 'gold button' was fabricated by electro-plating directly to the Au back contact of the diode. To be effective, the button had to be (a) sufficiently close to the junction for heat to reach it, (b) sufficiently large so as not to heat-up appreciably during the duration of the applied pulse. It had already been shown for a 3 microns thick layer of silicon, a pulse width greater than 500nS would result in a uniform temperature T_j from the junction to the base of the heat reservoir page 466 **[A1].** A thickness of 3 to 4 microns of silicon represented the limit of the technology in the 1970's. Equation (2) can be applied to the heat reservoir, by assuming the pulse-length was greater than 500nS. The calculations showed for a gold button thickness of 35 microns, and a pulse length of 5μS, the temperature of the gold button would reach $T \approx T_j/3$ at the end of the pulse, page 466 **[A1].** Significant improvements in the diode pulse thermal impedance were obtained by the inclusion of a gold reservoir on the back contact of the diode.

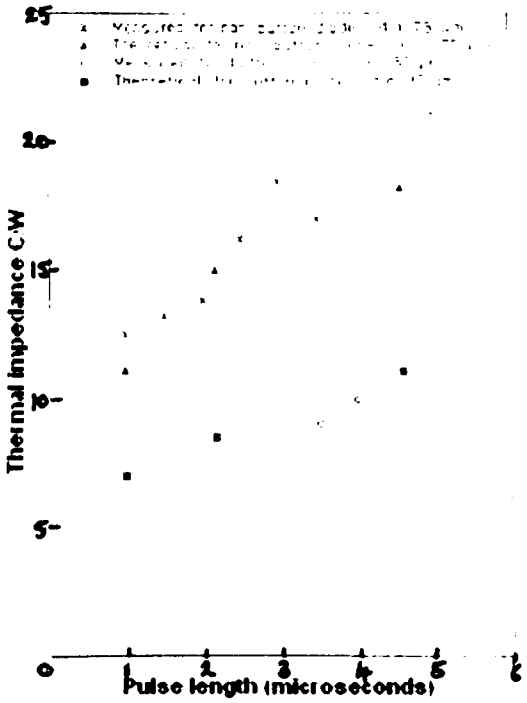


Figure 17: A comparison between experimental and theoretical values of pulsed thermal impedance

In Figure (17) is a comparison, carried out by the author, between experimental and theoretical values of pulsed thermal impedance of silicon TRAPATT diode of diameter 80 microns, with and without a gold-button. For practical diodes the silicon substrate was thinned to 7-8 microns by mechanical lapping and uniform thickness over the substrate was obtained by using thickness monitor holes **[A1]**.

Further improvement to the thermal impedance was obtained by using silver IHS technology **[I2]**, as silver has a higher thermal conductivity than gold. An experimental comparison of the thermal impedance between gold and silver heat-sinks for a range of device areas is shown in Figure 3, page 465 **[A1]**, which indicates approximately a 20% improvement in the CW thermal impedance using a silver integral heat-sink compared with gold. Still further improvements to the thermal impedance were obtained by the author by parallel connection of two (Figure 18) or three diodes **[A5]**, but was found to increase the parasitic inductive interconnection between the diode top-contacts, thereby severely limiting the performance at high frequencies **[I2]**. A photograph of a fabricated I-band TRAPATT diode with a gold-button heat-sink is shown in Figure (4), page 465 **[A1]**. The author adopted the simple 1D thermal model to calculate the thermal

impedance of a GaAs Read Impatt diode on diamond heat-sink, taking into account the change in thermal conductivity of the GaAs [I22].

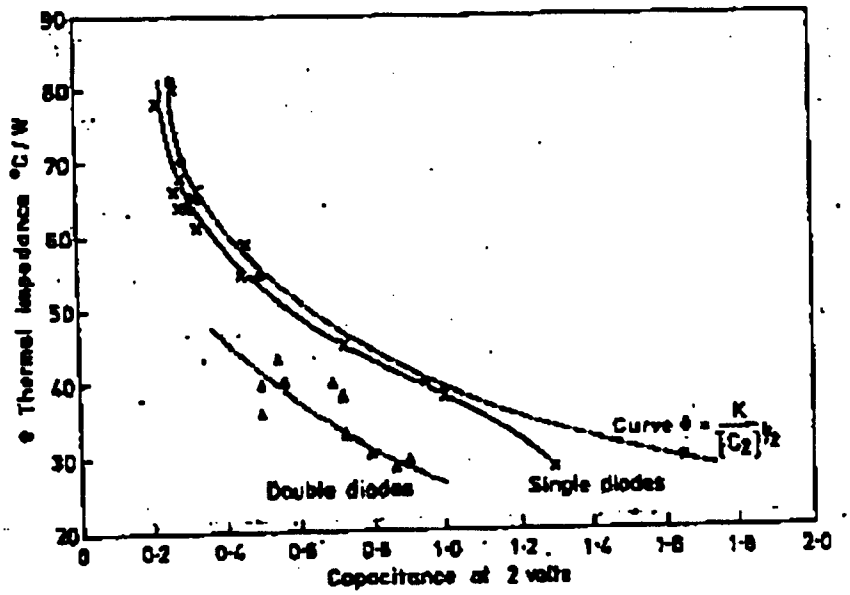


Figure 18: A comparison between the CW thermal impedance of single and parallel mounted diodes

2.7 Circuit Design

To obtain the desired RF output power the correct choice of diode capacitance had to be made. The diode was tested in a 50-Ohm experimental circuit therefore it was important that the diode was correctly matched to obtain the maximum power transfer. It was experimentally found by the author that the TRAPATT diode at its breakdown voltage had a junction capacitance in the range of 0.25-1.20pF, corresponding to diode junction areas from 0.3×10^{-4} to 0.8×10^{-4} cm^2 respectively [A1] and [I2]. The author found that the correct choice of diode capacitance had to be made depending on whether the device was to be used in an oscillator or amplifier configuration.

To operate the TRAPATT diode as an oscillator, it was mounted at one end of a 3.5mm diameter 50-Ohm coaxial air-line, which could support the pure transverse electric magnetic (TEM) mode to frequencies approaching $40GH_z$. The other end of the coaxial cavity could be connected to the RF test-bench via a 50 Ohm SMA connector. A diagram of the coaxial test cavity is shown in Figure 19.

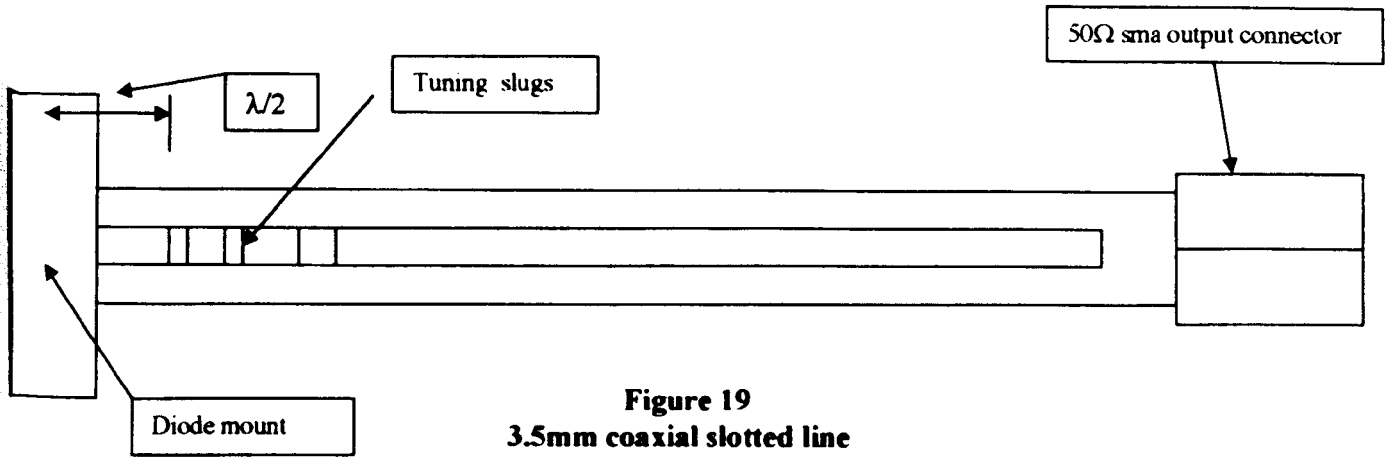


Figure 19
3.5mm coaxial slotted line

The 3.5mm coaxial line had a 1mm wide slot milled along its length to provide access to the tuning slugs and the line was gold-plated to minimise skin-effect loss **[A1]**. Moveable, low impedance 5 to 8-Ohm anodised aluminum tuning slugs between the diode and the 50-Ohm output of the coaxial line were used to match the diode and optimise the RF output power. The experimental work by the author indicated that the distance between the diode and the first tuning slug was slightly less than ½λ of the fundamental frequency, (page 312 **[A4]**) this had also been reported by Evans [20], which is a characteristic of the classical time domain triggered (t.d.t.) mode. Computer analysis carried out by the author showed that the relative positions of the slugs in the coaxial cavity did not equate to any of the more common low-pass filter functions, for example, Butterworth or Chebychev **[I2]**. The network appeared to be complicated, with the first slug closest to the diode acting as an impedance transformer at the fundamental frequency, while the remaining slugs provided reactive loading at the harmonics, (page 312 **[A4]**). The moveable tuning-slugs in the coaxial cavity precluded the use of the circuit in any practical application, other than bench-testing the RF performance of individual TRAPATT diodes. It was experimentally found that higher frequency of operation (J-band) could be obtained, by harmonic extraction, (page 27 **[A5]**). This reduced the complexity of fabricating TRAPATT diodes, which would be able to support the higher fundamental frequency of operation, and the subsequent design and machining of a coaxial cavity able to sustain TEM mode operation at approximately 80GHz. The

experimentally observed efficiencies and pulsed output powers of silicon TRAPATT diodes measured by the author from 2 to 18 GHz, are shown in Figure 4 and 5 respectively, (page 27 **[A5]**). The oscillator test circuit with moveable tuning slugs was used solely for identifying diodes with high RF efficiency and output power, from different diode process batches. The selected diodes were used in the more stringent amplifier circuits.

The amplifier circuit consisted of the 3.5mm diameter coaxial air-line, but with the tuning slugs of impedance between 10 to 20 Ohm, placed in different positions when compared with the positions of the tuning slugs in the oscillator coaxial cavity **[A4]** and **[A1].** Microstrip circuits were also designed and characterized by the author, but the maximum TRAPATT efficiency recorded was only 16% at 9.5GHz and therefore not pursued for this application **[I2].**

The TRAPATT diode was biased for Class C operation by setting the supply voltage just below its breakdown voltage. In this state the diode is switched-off. When a RF signal of sufficient amplitude is applied, the TRAPATT diode is triggered and the voltage drops below the bias voltage which enables a high current to flow through the diode, resulting in RF amplification **[I2, I3].** Biasing the diode below the breakdown voltage was achieved, either by using a synchronized pulse-generator to the RF input-source or by applying a dc bias below the diode breakdown voltage. The latter approach required a resistor and capacitor network in the bias-line, to absorb the diode voltage drop-back **[A3]** and was adopted in the amplifier circuits.

A novel rugged coaxial TRAPATT amplifier circuit was designed and developed by the author **[A1]** and **[I3],** which fulfilled the application requirements of vibration and shock Figure 4, page 467. The circuit was subject of UK patent **[A6]**.

The amplifier circuit consisted of metal plates with accurately machined central holes thereby reproducing the impedance of the coaxial line and tuning slug positions respectively. These plates were located by dowels and bolted firmly together **[I2, I3].** Fine-tuning was accomplished by shims to adjust the relative position of the matching sections. An internal dc block was developed as part of the inner coaxial line and the dc

bias was fed to the diode by an internal multi-section low-pass filter. The cavity could withstand a vibration of 23g RMS over a spectrum of 10 to 2000H_z without noticeable degradation in the RF output spectrum **[A1]**.

To meet the amplifier gain requirements a three-stage cascaded reflection amplifier **[I3]** utilising the TRAPATT diode was designed and developed by the author. The junction area of the diode was increased from the input stage (0.25-0.35pF) to the output stage (0.94 to 1.2pF) in order to manage the high output power requirement of each successive amplification stage. To minimise the RF losses and the overall size of the amplifier, a novel integrated microstrip circuit with circulators, isolators, dc feed-filters and dc breaks was designed by the author. The dc break between the amplifier stages consisted of a chip capacitor. While the low-pass bias-filter to bias each of the TRAPATT diodes consisted of chip capacitors and inductive wire links via gold-wire stitch-bonding. The completed microstrip circuit is shown in Figure 10, page 468, **[A1]**. The circulators and isolators were designed on lithium based ferrite substrates using in-house design software **[I3]**, which was developed and published **[A2]**. The microstrip assembly was mounted in an enclosure lined with microwave absorbent material to minimise box mode resonances **[I3]**.

2.8) Amplifier performance

The three-stage pulsed TRAPATT class C amplifier was RF tested and difficulties were experienced in obtaining the expected power added efficiency and gain from each amplifier stage **[I3]**. The problem was thought to be a result of poor harmonic isolation between stages. The isolation between stages was measured to be in excess of -50dB at the fundamental frequency of 9.7 GHz, but approached approximately -10dB at the second harmonic frequency, (page 469 **[A1]**). At the time of the research it was difficult to make s-parameters measurements at the higher harmonic frequencies. However, the inference was that each successive TRAPATT stage provided a degree of harmonic mismatch to the preceding TRAPATT stage thus contributing to noise and low gain

operation. It was found that the effects became more severe with increasing pulse-length as the impedance of the diode changed with temperature.

The TRAPATT diode junction temperature was found to rise rapidly with increased pulse-length causing transient impedance change, resulting in gain droop, reduction in efficiency and increased switch-on time **[I1 and I3]**

Experimental observation by the author showed that the increase in intra-pulse phase shift was directly proportional to pulse-length **[A1 and A5].**

A simple method of minimising both gain droop and intra-pulse phase shift with increasing pulse width was developed. It consisted of an electronic compensation circuit, which derived its switch-on trigger from the voltage drop-back across the diode and switch-off trigger when the source voltage recovered. Therefore, the trigger circuit was only instigated during the RF input signal to the TRAPATT diode. This enabled a variable exponential current source to be superimposed on the current being drawn from the constant voltage supply, enabling shaping of the current waveform to the diode. Significant improvements were obtained, and for example, the amplifier gain was increased by 12 to 20%, and the intra-pulse phase shift reduced from 70^0 to 30^0 **[I3].**

The complete three-stage amplifier gave a gain of 9 to 10dB with a peak output power in excess of 10 watts, with an overall added power efficiency of approximately 7% for pulse widths between 0.5 and 1.0 microseconds, at the centre frequency of 9.7GH_z. The supply voltage to the amplifier was 36Volt.

The three-stage class-C TRAPATT power amplifier was driven by state-of-the-art 500mW power FET amplifier. A photograph of the complete assembly is shown in Figure 13, page 470, **[A1].**

2.9) Conclusions

The research work concluded that a solid-state TRAPATT power amplifier had a unique voltage drop back characteristic which enabled it to work in class C operation, with the potential of high added power efficiency. The amplifier was shown to work from a low voltage (36V) DC source, thus suitable for airborne applications. Amplifier operation was

feasible in I-band, but, the design would be very difficult to manufacture, as the circuit had to provide resistive match at the fundamental and phase matched short circuits to at least the 4th harmonic (> 40GHz). The interaction between the diode and circuit in the amplifier mode was sensitive to an individual diode, and the operation of the mode was not fully understood which could be a subject of further research **[I3].** This made the circuit design difficult to reproduce reliably and was only feasible by experimentally fine tuning each individual amplifier-stage to a particular diode. The inter-circuit stages also had to provide a high RF isolation (>50dB) between the successive gain stages, and over a wide frequency range i.e. 40 GHz.

The research work clearly showed that although, in I and J band, high peak oscillator powers and efficiencies could be obtained in the laboratory, they were not feasible within a manufacturing environment. Leading to the conclusion that the device would be more usefully used in applications at lower microwave frequencies (L and S –band) where the device and circuit requirements were far less stringent.

During this period of research and development of the TRAPATT power amplifier, the performance of power MESFET improved significantly **[B8**, 21] and commercial X-band power transistors were becoming available [22], which would eventually enable the original power amplifier specification to be met with the potential of good manufacturing reproducibility.

A number of industrial organisations have continued work on the TRAPATT diode for low frequency applications (L and S-band) where the device and circuit reproducibility can be obtained more easily [23]. In particular, the high RF pulsed-power and efficiency at L-band, make the device directly applicable to microwave proximity fuses.

An alternative approach in obtaining a source of high RF pulsed output power and at high frequencies (X-band or J-band) is by power combining locked oscillators. The locked-oscillator approach was investigated by the author using the TRAPATT technology **[A5 and I1]** and the results are shown in Figure 20.

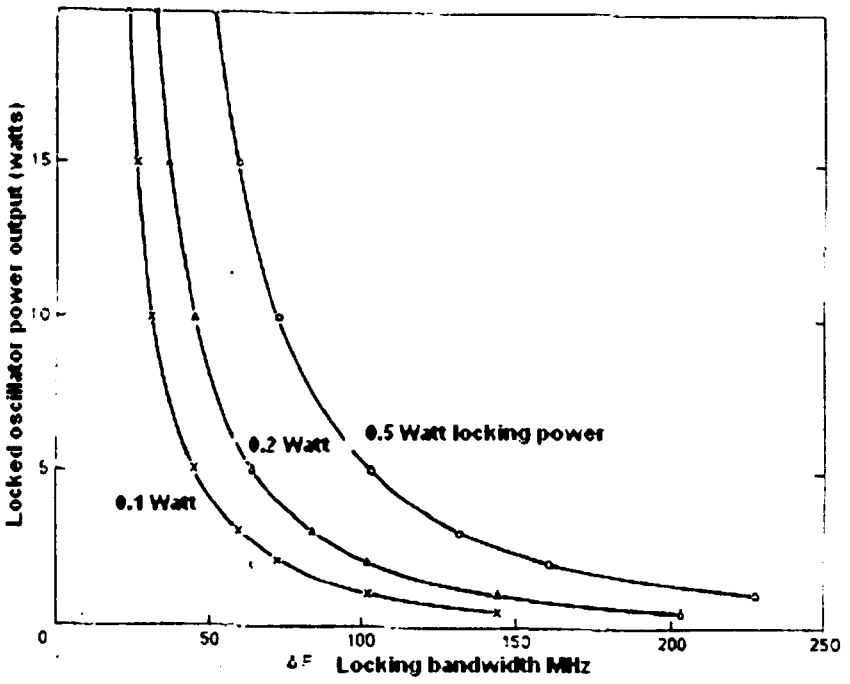


Figure 20: TRAPATT locked oscillator

A more complete study was carried out using Indium Phosphide (InP) transfer electron diodes (TED) **[A7]**, as they were easier to use at the higher microwave frequencies (X to J-band). It should be noted that the devices were operated with short pulse lengths and low duty factors < 0.1%, when compared with the TRAPATT diode, as the device dc to RF conversion efficiency is much less than that of a TRAPATT diode.

The study on combining locked InP TED oscillators, carried out by the author, clearly indicated severe bandwidth problem's **[A7]**, again due to the frequency chirping across the pulse as a result of the thermal excursion. The work indicated that by combining two locked oscillator sources using a single-stage of a tree combining network [24], a realistic band-width in J-band was only 1-2% of the fundamental frequency. Clearly, if TRAPATT devices were used the bandwidth limitations would be more severe, as is shown in Figure 20, which was for a single locked oscillator operating at a fundamental frequency of 10 GHz.

The above work has indicated major problems in using two terminal devices for high output power and over wide bandwidths. The two-terminal device (TED) appeared to be

more suited for single frequency or narrow bandwidth high-power applications. Further, as already stated, the mechanism for generating microwave output power in avalanche diodes is not conducive in obtaining low noise figures. Therefore, other technologies, for example the GaAs MESFET were investigated.

INDUSTRIAL REPORTS supporting the work I1, I2, I3, I4, I22.

CHAPTER 3): THE GALLIUM ARSENIDE METAL SEMICONDUCTOR TRANSISTOR (MESFET)

3.1 Introduction

In 1965 the first microwave gallium arsenide (GaAs) metal Schottky barrier field-effect transistor (MESFET) was fabricated and measured at the Plessey Company Allen Clark Research Centre [25]. By 1971, one-micron gate-length GaAs MESFETs were being fabricated with an f_{max} of 50GHz and a f_t in excess of $20GH_z$ [26]. These represented substantial improvements over silicon, primarily due to the high mobility of electrons in GaAs (six times higher than in silicon) and the very high peak electron saturation drift velocity [27]. Also, the GaAs active layer could be grown on a semi-insulating GaAs substrate with a resistivity greater than 10^7 Ω cm, thus the large parasitic capacitance normally associated with the gate bonding-pad was removed by positioning the pad on the substrate. The reduction in the parasitic capacitance enabled the higher cut-off frequencies to be obtained using existing structures. The high resistivity substrate also paved the way to microwave monolithic integrated circuits (MMIC) [28]. Over the next three decades considerable development of the FET took place and a number of variants emerged. These included the HEMT (high electron mobility transistor) [29], VMT (velocity modulation transistor) [30], CHINT (charge injection transistor) [31], TWT (travelling wave transistor) **[B12],** [32] and LGT (linear gate transistor) **[B9].**

The HEMT, without doubt, has been the most significant advancement in FET technology. In the MESFET, the carrier electrons in the conducting channel are introduced by doping the semiconductor channel with donor impurities. These impurities act as scattering centres on the carrier electrons thereby reducing their mobility. In the gallium aluminium arsenide/gallium arsenide (GaAlAs/GaAs) HEMT, the electrons are provided by the n-type GaAlAs layer but are constrained by the potential barriers at the GaAlAs/GaAs interface to conduct in the undoped GaAs layer. As the GaAs layer is undoped, the electron carriers gain higher mobility in comparison with a conventional MESFET. To-date, cut-off frequencies have been reported for GaAlAs/GaAs HEMTs in

excess of 200GH$_z$ for a gate length of 0.12 microns [33] which is considerably higher than for a conventional MESFET with the same gate-length [34].

The FET has almost completely displaced the two terminal solid state devices (TRAPATT, TED and IMPATT diodes) in many applications, and in recent years has encroached into the milli-metric frequency applications (40 to >100GH$_z$) [35,36]. It is still fair to say that at milli-metric wave frequencies where high power, narrow bandwidth and low cost are required, two terminal devices (IMPATT and TED) still offer viable solutions. For example, the 77 GHz automotive collision avoidance radar, the GaAs Gunn diode is very competitive in terms of cost and performance when compared directly with the FET technologies in the form of microwave monolithic integrated circuits (MMIC) **[C5]**. This may only be a transient phase, while the MMIC cost remains high due to relatively low numbers of circuits required at 77 GHz and higher frequencies.

The research work presented was carried out by the author, who was the team leader of a small group of research scientists and technologists, at the Plessey Allen Clark Research Centre between 1980 to1986. The work was significant in the development of the milli-metric MESFET for low noise performance **[I23]**. The work also contributed in paving the way in laying the foundation for the rapid development of the high electron mobility transistor (HEMT). Many of the design features, in particular the device geometry and techniques in RF-characterisation developed by the author, are directly applicable to the HEMT and are currently in use today.

The Allen Clark Research Centre, Caswell, UK, was the home of the GaAs MESFET [37], and held a world-wide lead in the development of the millimetric wave MESFET during the 1980's. In 1980 devices were being fabricated on material grown by vapour phase epitaxial (VPE) technology, with gate lengths of 0.3 microns **[I5,I6,I7,I8]** realised by electron beam (EB) lithography [38, 39]. These devices had a measured NF_{min} = 4.8dB with an associated gain G_a of 4.8dB at 28GHz **[B7]**, [40]. The summarized research work led to MESFET devices with an NF_{min} = 2.6 dB and G_a = 5dB at frequencies in excess of 32 GHz **[B2]**. These were successfully used in INTELSAT (contract nos INTEL173) **[I19]**, and ESA (contract nos 4490/80/NL/MS) **[I20, I21]** space applications. Both research contracts required a level of device qualification **[I19]**, which

had not been carried out to any extent on MESFETs utilizing the relatively new narrow EB gate technology. The author will also describe how the above device research lead to the invention of the LINEAR GATE TRANSISTOR (LGT) [B9] and subsequent improvements in the GaAs power MESFET technologies [B8,I13].

3.2 Transistor design

A simple schematic plan view of a single-cell of a MESFET is shown in Figure 21.

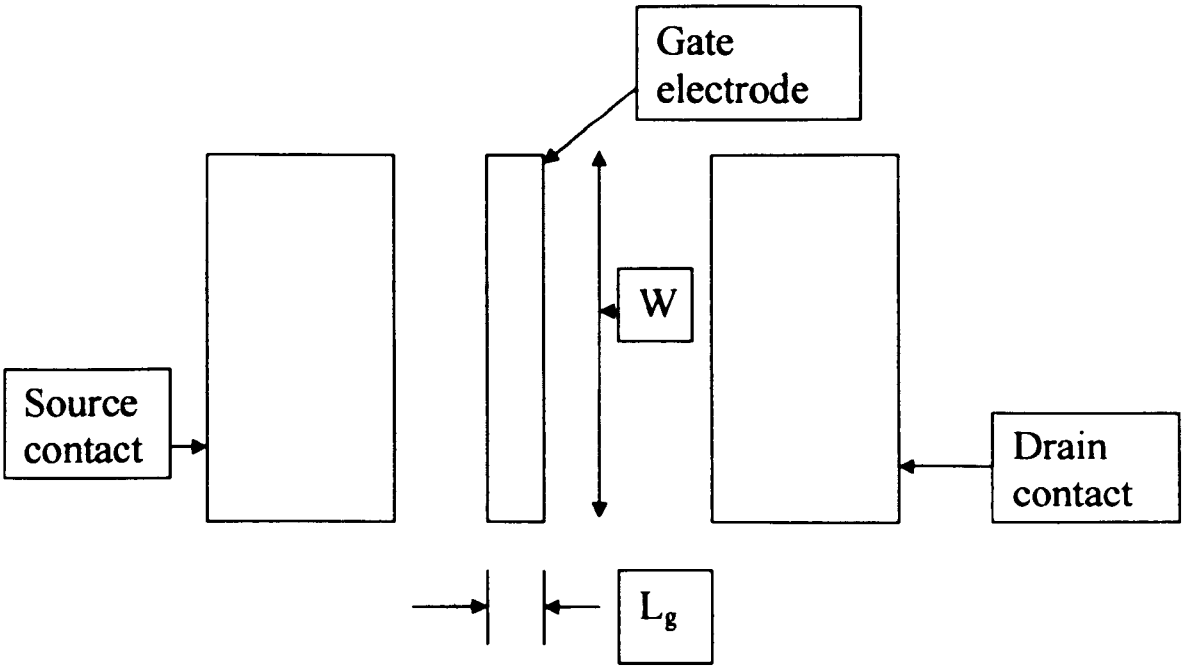


FIGURE 21 SCHEMATIC of a SINGLE CELL FET

The cell consists of three electrodes, which are known as the source, gate and drain. The gate length (L_g) determines the frequency of operation, while the gate-width (W) determines the impedance and output power capability of the transistor. The cut-off frequency (f_t) of the MESFET may be very simply thought of as being inversely

proportional to the carrier transit time under the gate. Therefore, to a first approximation to realize a high frequency of operation, a short gate-length and a semiconductor material where the carriers have a high a saturation velocity are required. The above also assumes an ideal semiconductor substrate interface. Unfortunately in reality defects exist in the semiconductor/substrate interface which increase scattering of the carriers and particularly at high electric fields providing a parallel conduction path to the channel, thereby reducing the current modulated by the gate.

As the gate-length is shortened, the thickness of the semiconductor active region has to be reduced and the carrier concentration increased in order to preserve the pinch-off characteristic (V_p). It should be noted that the higher carrier concentration degrades the gate drain breakdown (VB_{DG}) of the transistor [41]. While a reduction in the active semiconductor thickness will lead to a higher parasitic source (R_s) and drain (R_d) resistance, and higher gate source capacitance, (C_{gs}) reducing the extrinsic transconductance (g_{me}) of the transistor. Often the gate electrode is displaced towards the source contact (Figure 8) to reduce the parasitic source resistance as this parasitic source appears directly in the feedback loop and can significantly reduce the extrinsic transconductance g_{me} [42]. For the same reason the reactance (X_L) of the parasitic source inductance L_s, for making contact between the source electrode and ground, becomes very important at high frequencies.

Stringent requirements are required of the semiconductor material to maximise the intrinsic transconductance g_{mi} of the transistor and are summarised below:

a) An abrupt step in the carrier concentration at the substrate interface to maintain the transconductance of the transistor over the complete operating range of gate-source voltage V_{GS}.

b) A minimum number of traps, defects and material imperfections at all semiconductor interfaces, as these degrade the carrier transport mechanisms (mobility of carriers), thereby reducing the speed of the transistor.

c) A high resistivity substrate (ideally non-conducting) to minimise un-modulated leakage current in the substrate, which will degrade g_{mi}. The leakage current can start to become significant in small geometry devices required for high-frequency of operation **[50].**

Experimental transistors with gate-lengths of 0.3/0.2 microns (measured by scanning electron microscope: SEM) were fabricated by a hybrid photolithography / electron-beam lithography process using a lanthanum hexaboride electron beam source [43]. The n-type active layer was grown by vapour phase epitaxy on a high resistivity (10^7 Ohm-cm) buffer layer **[B1].** The fabricated transistors had a high transconductance and good pinch-off characteristics, indicating a high quality semiconductor/substrate interface.

Some initial experiments were carried out using metal organic chemical vapour deposition (MOCVD) in order to investigate the growth of a wide-band gap material gallium aluminium arsenide (GaAlAs) between the active GaAs layer and the substrate. The GaAlAs acted as a potential well to further reduce the leakage of carriers into the substrate **[B4].** The measurements on these devices carried out by the author showed little or no improvements over devices fabricated directly on the high resistivity substrate; it was thought that the purity of the wide band-gap material at that time was not sufficiently good to see the expected improvements. Hence this option was not continued in the present reported work.

In Table 3 shows the experimental values measured by the author (unpublished) for a number of transistor parameters including the extrinsic transconductance (g_{me}), source resistance (R_s), gate source capacitance (C_{gs}), drain source resistance (R_{ds}) and the minimum noise figure (NF_{min}) as a function of the active carrier concentration in the channel region. The total gate-width of the transistor was 100 microns with a gate-length 0.3 microns and the semiconductor was grown by VPE on a high resistivity buffer layer.

TABLE 3

Active layer carrier conc. (atoms/cm^3)	g_m (mS)	R_S (Ohms)	C_{gs} (pF)	R_{ds} (MΩ)	NF_{min} (dB) 14 GHz
$2.0x10^{17}$	11.0	14.0	0.08	1.0	1.8
$3.0x10^{17}$	13.0	10.0	0.10		
$3.5x10^{17}$	15.0	8.5			1.7
$3.7x10^{17}$	20.0	7.5	0.13	1.3	1.6
$4.0x10^{17}$	23.0	6.0	0.15	1.6	1.3

The above information enabled the selection of the optimum carrier concentration, and a number of transistor geometrical configurations for high frequency operation were then investigated. The structure with a 'pi–geometry' and trapezium shaped source-electrodes was finally selected by the author **[I7, I19]** , and this became known as the C1 device, see Figure 1, page 335 **[B2].** This geometry has remained almost untouched as the test vehicle to the present-day, and was recently used by Marconi Research for investigating HEMT devices fabricated on Gallium Nitride GaN [44].

The major electrical parameters considered in the design were the source inductance (L_s), source resistance (R_s), gate resistance (R_g), and intrinsic transconductance (g_{mi}).

3.2.1 Source Inductance (L_S)

To obtain the maximum available gain (MAG) at high frequencies from the transistor, the source inductance required to be minimised. The C1 transistor design with the trapezium shaped source electrodes, allowed the bonding of short multiple wire-bonds, or tape

bond, thereby minimising the parasitic source to ground inductance. The 'mesa' (the active layer) was also designed to be outside of the source-pad outline to provide a planar bonding area **[B7]**. The gate metallisation was widened over the mesa edge to avoid current crowding **[B7]**. Theoretical modelling carried out by the author indicated that the C1 transistor with external tape-bonding would have an inductance of approximately 0.015nH similar to a device with plated source wrap-round contact, or 'via' contact. The effect of source inductance on the high frequency gain is shown in Figure 11, page 100, **[B4]**. Note the source bonding pads had a small geometrical parasitic C_{gp} capacitance associated with them, which reduced the $f_t \approx g_{mo}/2\pi(C_{gs} + 2C_{gp})$ [45] of the transistor.

3.2.2 Source Resistance (R_S)

To minimise the total source to gate (R_S) and gate to drain (R_D) parasitic resistance the author adopted a number of design features, which included the self-aligned etched channel gate technology (Figures 5 and 6, page 99 **[B4]**) and a thin high doped n^+ ($\sim 10^{18}$atoms/cc) layer grown directly on the n-active region **[B2, B4]**. To obtain good pinch-off characteristics the gate-length to active layer thickness aspect ratio was found to be the order of three, which was in agreement with the Pucel model [46]. The transistors were fabricated using a positive high contrast electron-beam resist [47], which resulted in steeper channel sides (reducing the undercut) and subsequently lower source and drain parasitic access resistance to the channel. The experimental measurements made by the author, of the total source $R_S = R_C + R_S^1$ and drain $R_D = R_C + R_D^1$ resistance were of the order of 0.5 to 0.8Ω/mm respectively **[B4]**, and represented the state of the art figures in the mid 1980's. R_C represents the metal/semiconductor ohmic contact resistance. Modelling work carried out by the author indicated that an increase in the parasitic source resistance resulted in a small decrease in the high-frequency gain, but a significant increase in the minimum noise figure NF_{min}. Figure 22 shows the experimental performance of the minimum noise figure at 14 GH_z of the C1 transistor as a function of source resistance R_S. The effect of the parasitic source inductance L_s on the high-frequency (32GHz) minimum noise figure (NF_{min}) was calculated using the Fukui noise theory [48] and plotted in Figure 11, page 100 **[B4]**.

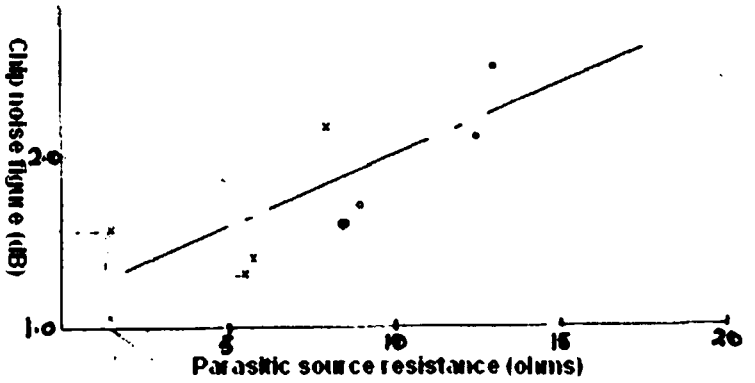


Figure 22: NF_{min} versus parasitic source resistance R_s at 14GHz

3.2.3 Gate Losses (R_g)

To maximise the high-frequency gain and minimise the noise figure, the transistor intrinsic cut-off frequency $f_t = (1/2\pi)[g_{mi}(C_{gs} + C_{gd})]$ is required to be as high as possible. Therefore, both the gate source (C_{gs}) and gate drain (C_{gd}) capacitance required to be minimised. For the C1 transistor the f_t was estimated to be $60GH_z$. This was primarily obtained by reducing the gate-length to nominally 0.25 microns. The maximum unit gate-width for a transistor was determined by the onset of RF transmission distributed effects along the gate. Hence, to raise the frequency of operation of the device both the gate length and width had to be reduced. Figure 7, page 338 **[B2]** shows the effect of reducing the unit gate-width on the minimum noise figure with respect to frequency, for a constant gate-length of 0.3 microns. As the gate length is reduced the resistive losses of the gate increase. The resistive loss is a function of the gate metal conductivity, gate-length, and gate metallisation thickness, which is governed by the depth of the gate channel and the thickness of the resist layer. The minimum noise figure for the C1 device structure was calculated at 24 GHz using the Fukui model and plotted as function of gate-metallisation, Figure 9, page 39 **[B2]**.

The gate metallisation thickness can be further increased by a 'wide-head' T-shaped gate profile, thus substantially reducing the resistive loss. This technology will be discussed in sections (4.4 & 4.5) with reference to the travelling wave FET. Very recent published work by Onodera [49] 1999, has shown that ultra low noise performance can be obtained from a GaAs MESFET using a short gate-length (0.12 μm) with a T-shaped gate profile, to minimize the parasitic gate resistance.

Note that a gate bonding-pad, which is outside of the mesa area, provides a small parasitic geometrical capacitance C_{gp} and the thin metallised gate stripe would have a high parasitic self-inductance L_g, which is dependent on the depletion layer thickness under the gate [50].

From the preceding analysis, it may be deduced that improved RF performance can be obtained by going to very short gate-lengths. To investigate this effect, some work was undertaken in collaboration between the author and Glasgow University. Devices were fabricated on Plessey VPE material, grown on a high resistivity buffer layer. The gate-lengths were fabricated at the University of Glasgow using electron-beam lithography and with gate-lengths varying between 0.21 to 0.055 microns [50]. The measured dc characteristics showed reasonable extrinsic transconductances g_{me} of around 300mS/mm, but the devices with the very short gate-lengths had very poor pinch-off characteristics even at low drain source voltages, of less than 1 Volt. The work undertaken by Glasgow University indicated that the expected increase in the high-frequency performance of the transistor was not obtained by reducing the gate-length to very small dimensions. Further, the work at the University of Glasgow suggested the poor pinch-off charactersistic was probably due to an increase in the charge leakage through the buffer layer as a result of the smaller geometrical dimensions. The leakage current was also found to be a function of the drain source voltage [50]. It was concluded that to overcome the problem of fabrication of very short gate-length transistors, high quality material and abrupt interfaces between the active GaAs layer and the undoped high resistivity buffer layer was required, possibly by the inclusion of a wide band-gap material. To successfully grow the above material specification molecular beam epitaxy (MBE) or MOCVD technologies were required.

It is interesting to note that all high frequency, narrow gate-length devices are now fabricated on MBE or MOCVD grown material with heterojunction buffer layers [51].

3.2.4 Transconductance (g_m)

The gain of the transistor is partially governed by the magnitude of the extrinsic transconductance (g_{me}). The $g_{me} = g_{mi}/[1+g_{mi}R_s]$ is a function of both transistor geometry and material parameters. If the device geometry is maintained, the transconductance may be improved by increasing the carrier concentration. This, however, will reduce the drain-gate breakdown voltage VB_{DG}, increase the pinch-off voltage V_P and input capacitance C_{gs}. Hence, in practice a compromise in the level of carrier concentration is required. The intrinsic transconductance (g_{mi}) can also be further improved by reducing the defects in the semiconductor material to minimize any parallel conduction paths with the device channel.

The C1 transistor was fabricated with a 0.25 micron gate-length on GaAs material with a n^+ contact layer, high active carrier concentration grown on a high resistivity buffer layer, giving a low source resistance R_S resulting in an extrinsic transconductance g_{me} of 250 to 320mS/mm **[B2, B4].**

The preliminary RF results of the C1 structure were first published in the IDEM 1981 conference in Washington; with a NF_{min} of approximately 4 dB at 30GH_z, see figures 6 and 7 page 683 **[B7].** (The results are cited in Shur's book on 'GaAs Devices and Circuits' [33] as some of the first open published MESFET high frequency noise measurements).

A further design iteration of the C1 structure led to enhanced microwave performance, with a NF_{min} of 2.6 dB at 33GHz **[I8 &I19]** published in 1986 **[B2, B10].**

3.3 DEVICE MODELS

To optimise the transistor design for both high frequency gain and minimum noise figure (NF_{min}), a transistor equivalent circuit model was developed based on empirical data obtained at dc and microwave frequencies to 18 GH_z. The equivalent circuit model

consisted of the electrical equivalent circuit of the intrinisic FET with parasitics (R_g, R_s, R_d, L_s, L_d, L_g, C_{gp}, C_{sp} and C_{pd}) [I7] attached to form the electrical extrinsic model, see Figure 23.

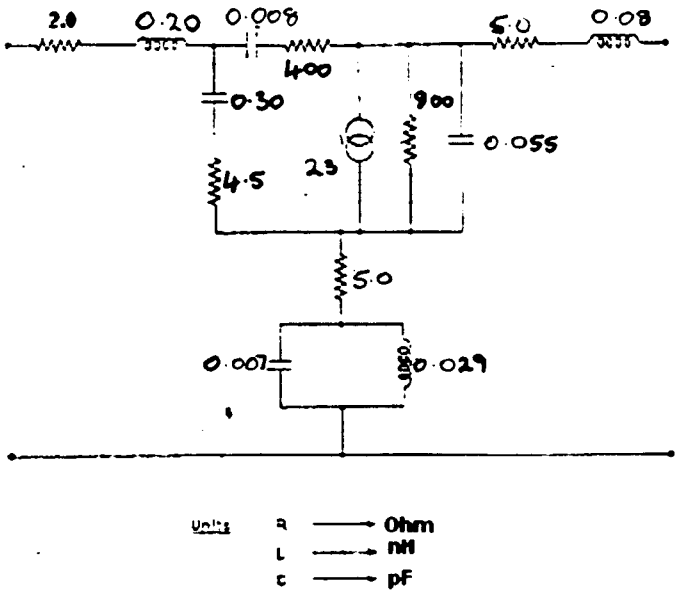


Figure 23: Equivalent circuit model

3.3.1) DC Characterisation

A computer controlled probe station was available to probe individually numbered chips across the wafer [I5]. Histogram plots of the measured parameters (I_{DSS}, V_P, g_{me}) were obtained for each fabrication batch, an example is given in Figure 14, page 101 [B4].

Individual chips could be selected with high extrinsic transconductance and gate-drain breakdown voltage (typically 10V) and good pinch-off characteristics. These were bonded on to single ceramic 50-Ohm microstrip test circuits. These circuits were used to obtain dc measurements of the parasitic source (R_S), drain (R_D) and the intrinsic channel resistance (R_I) using the method of Hower and Bechtel [53]. The typical measured parasitic source resistance was between 0.6 - 0.8 Ohm/mm and knowing the extrinsic transconductance for a particular bias condition an estimate of the intrinsic $g_{mi} = g_{me}/(1-g_{me}R_S)$ could be found. The gate-length and position of the gate with respect to the source

contact were measured using the scan-electron microscope. From these measurements an estimate of the gate resistance could be made using [54]:

$$R_{gdc} = w_{unit}^2[2\pi\rho\mu F]^{0.5}/[3L_g W\sqrt{2}] \qquad (3.3.1.1)$$

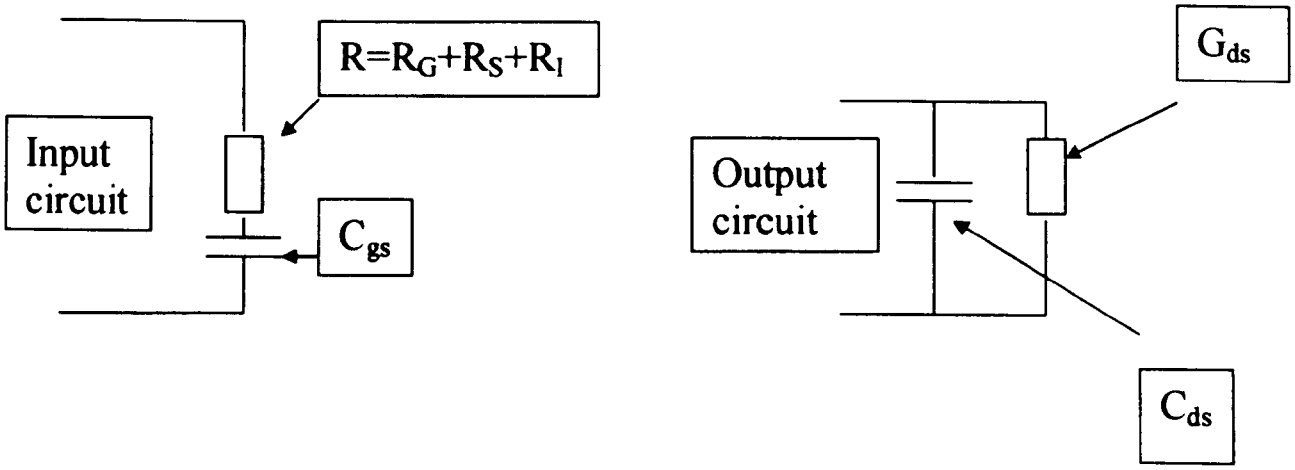
Where ρ is the gate metal resistivity, L_g gate length, μ gate metallisation permeability, W total gate width and w_{unit} is the unit gate width and F frequency of operation. Note the factor 3 in the denominator accounts for distributed resistive effects along the metallised stripe.

3.4 RF ASSESSMENT and PERFORMANCE of the TRANSISTOR

3.4.1 Microwave frequency measurements

The minimum noise NF_{min} measurement at 14 GH_z was carried out on all batches of transistors, and provided NF_{min} was less than 1.5dB, the batch was RF characterised at high frequencies **[I8].**

S-parameter measurements (2 to 18 GH_z) of the transistor were made at the low noise bias condition (10% of Idss). The device was mounted in a 50-Ohm microstrip circuit enclosed in a box with a cut-off frequency in excess of 18 GH_z. The circuit parameters (microstrip launchers, 50-Ohm microstrip line, and bond wires) were de-embedded from the measured s-parameters. From these measurements, the input and output unilateral models (Figure 24) of the transistor were derived and along with the dc measurements enabled the small signal extrinsic equivalent circuit model to be obtained at the low noise bias condition **[I5].**



INPUT CIRCUIT (C_{gs} gate/source capacitance, R total input resistance)

OUTPUT CIRCUIT (C_{ds} drain/source capacitance, G_{ds} output conductance)

Figure 24 (Unilateral Model)

Other circuit parameters, such as, the bonding-pad capacitances (C_{gp} and C_{dp}) were calculated from geometrical dimensions of the transistor.

3.5 TRANSISTOR DEVICE MODELS

3.5.1 Equivalent Circuit Lumped Element Models

The microwave frequency and dc measurements enabled the author to develop an extrinsic equivalent circuit model of the transistor, which would bear some resemblance to the physical model of the device. It was found experimentally, by the author, that if the measured dc parasitic R_S and R_D resistances were fixed, and the measured intrinsic parameters (C_{gs}, C_{ds}, R_{ds} and g_{mi}) were fine tuned, the estimated parasitic elements (C_{gd}, R_g, L_g, L_d, L_s and C_{PAD}) could then be tuned to fit the electrical equivalent circuit model to the measured s-parameters, to 18GH_z. This approach maintained as far as possible the physical aspects of the device, giving some confidence in extrapolating the model to higher frequencies 40GHz. The equivalent circuit of the C1 transistor is given in Figure

10, page 100 **[B2].** The modelled s-parameters (s_{11} and s_{22}) were extrapolated to 32 GHz, and directly compared with measurements by the author using the slotted-line and reasonable agreement was obtained. This gave further confidence in being able to extrapolate the s-parameters to high frequencies from the electrical equivalent circuit model. The comparison is shown in Figure 2, page 261 **[B5].** Further, the experimental maximum available gain (MAG) was compared with the MAG calculated from the extrapolated s-parameters to $40GH_z$, and good agreement was obtained, in Figure 13, page 100 **[B 4].**

The above outlined method required an estimation of the value of the feedback capacitance C_{gd}, a starting order of value was obtained from simple geometrical calculations. The more recent work of Cappy [55] and Pritchett [56] using Y-parameter de-embedding, enables the feedback capacitance C_{gd}, the pad capacitance's C_{ps}, C_{pd} and gate-source leakage conductance g_{gs} to be extracted directly from s-parameter measurements. The above method has been adopted and further refined in the GaN modeling, reported in section 5.0 of this thesis.

3.5.2 Distributed Circuit Model

At high frequencies other physical effects were found to become important in the multi-finger transistor and must be taken into account to adequately describe the transistor. These effects include inter-electrode coupling, giving rise to additional parasitic capacitance and mutual inductance, and distributed phase effects along the metallised gate stripes.

A unit section of a conventional MESFET can be viewed as three coupled active transmission lines, see Figure 25.

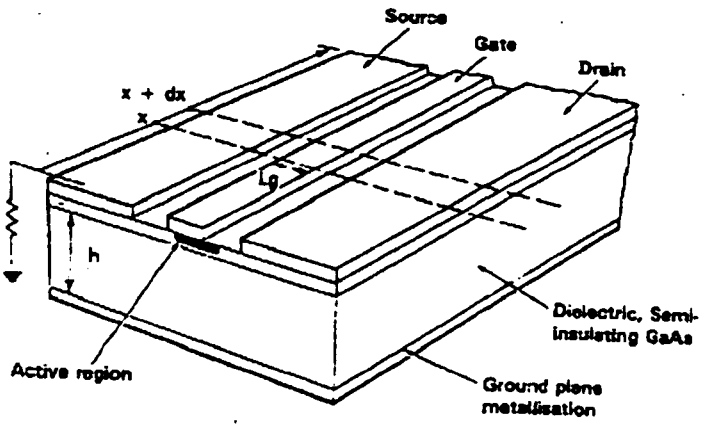


Figure 25, Coupled electrodes

Superimposed onto the inter-electrode capacitance and inductance is the active FET device, which may be considered as a distributed intrinsic FET equivalent circuit model. The solutions were limited to the transverse electric mode (TEM) and resulted in 6 normal modes, with three travelling in each direction along the width of the device. By solving the problem for the C1 pi-structure (S-G-D-G-S) which is a five-coupled active transmission line problem with ten normal modes page 336 **[B2]**. The distributed model for a pi-FET with unit gate width of 50 microns and a gate-length of 0.25 microns was used to calculate the s-parameters to $40GH_z$. The s-parameters were then compared with the s-parameters for the same device but modelled as the lumped electrical equivalent circuit model. Good agreement was found at low frequencies with an increasing deviation as the frequency increased. The departure between the two models was dependent on the unit gate width. The larger the magnitude of the unit gate-width the lower the frequency at which the two models diverged. The frequency at which the two models diverged was considered to be the point of differentiation between representing the transistor as a lumped or distributed network. The comparison of the above results was published in reference **[B2]**.

3.5.3 Noise Figure Model

The noise performance of a FET device is primarily determined by the diffusion current flowing in the channel which can be represented by noise current source i_d, and i_g is related to the noise current induced in the gate circuit by charge fluctuations in the drain circuit. Therefore, i_g and i_d are correlated. The remaining noise sources are primarily due to the extrinsic parasitic elements which dissipate power giving rise to thermal noise. For example, the gate resistance R_g, and the source resistance R_s these can be represented by noise voltage sources. The parasitic drain resistance R_d follows the intrinsic FET and its effect can normally be assumed to be negligible. The model can be extended by also considering gate leakage effects due to shot noise and these will not be correlated with the gate noise due to channel fluctuations. The effect of gate leakage noise will be considered in more detail in section 5.3.

Purcel [58] developed a physical model for the FET transistor by considering the separate noise contributions as outlined above, and assuming the gate leakage noise was negligible. The Purcel model is fairly complex and experimental work by Fukui [57] indicated that very reasonable agreement between the model and experiment could be obtained by neglecting the noise contribution i_g in the gate circuit. This greatly simplified the noise model.

Therefore, the semi empirical Fukui Noise Model [57] was extensively used to investigate the effect of the different device parameters on the minimum noise figure (NF_{min}) of the transistor. The model is particularly useful, as it is conceptually simple, and the parameters still bear a direct physical description of the transistor.

As already stated the model is an approximation of the more general expression for the minimum noise figure of an intrinsic MESFET given by Pucel physical noise model [58]:

$$NF_{min} = 1+2(2\pi FC_{gs}/g_{mi})[K_g(K_r + g_{mi}(R_g + R_s)]^{0.5} +$$

$$2(2\pi FC_{gs}/g_{mi})^2[K_g g_{mi}(R_g + R_s + K_c R_l] + ... \qquad (3.5.3.1)$$

Where $K_g = P[(1-C\sqrt{R/P})^2 + (1-C^2)R/P]$ and (3.5.3.2)

$$K_r = R(1-C^2)/[(1-C\sqrt{R/P})^2 + (1-C^2)R/P] \quad (3.5.3.3)$$

R and P are the drain and gate noise coefficients respectively and are dependent on the bias conditions and transistor geometry. The coefficients R and P are related to the noise sources $\langle ig^2 \rangle = 4kTG_iR\Delta F$ and $\langle id^2 \rangle = 4kTg_{mi}P\Delta F$ respectively.

$C = \dfrac{< ig > . < id >}{(< ig^2 > . < id^2 >)^{0.5}}$ is the correlation factor and describes the link between the gate and drain noise sources. The drain noise $\langle id^2 \rangle$ is normally the most significant of the noise sources and is dependent on the channel diffusion current. From equation (3.5.3.1) it is seen that the gate noise $\langle ig^2 \rangle$ influences the drain noise $\langle id^2 \rangle$ even at very low frequencies as the two noise sources are correlated.

It should be noted that if the gate noise is considered to be negligible, and therefore, there can be no correlation between the gate and drain noise sources, hence R = 0 and C = 0. Further, if all the higher order terms are neglected, the Purcel equation (3.5.3.1) reduces to:

$$NF_{min} = 1+2(2\pi FC_{gs}/g_{mi})[\, Pg_{mi}(R_g + R_S)]^{0.5} \quad (3.5.3.4)$$

This is the Fukui equation and is independent of gate bias and $P = (K_F/2)^2$ where K_F is the Fukui empirical coefficient. Hence:

$$NF_{min} = 1+K_F(2\pi FC_{gs})[(R_g + R_S)/g_{mi}]^{0.5} \quad (3.5.3.5)$$

Further, if the assumption is made that the gate voltage is zero, $\langle id^2 \rangle$ is then characterised by the thermal noise generated in drain conductance G_{ds}, and it can be shown that $P = G_{ds}/g_{mi}$ [59].

The Fukui expression can then be rewritten as:

$$NF_{min}=10\log\{1+2\pi K_FC_{gs}F[((R_{S1}+R_{S2}+R_C)+R_g)\,/g_{mi}]^{0.5}\text{dB} \quad (3.5.3.6)$$

Where:

C_{gs} = gate-source capacitance

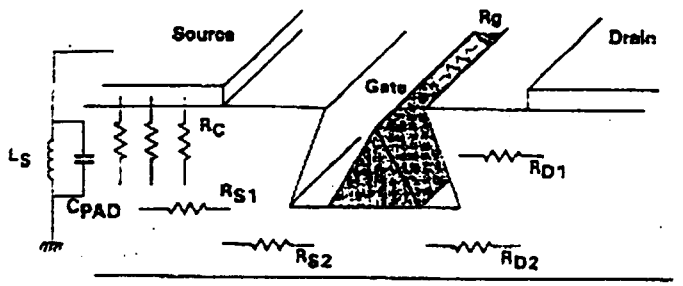
F = frequency

$R_{S1}+R_{S2}+R_C$ are the resistive components of the total source resistance R_S. Where R_C is the metal semiconductor ohmic contact resistance, R_{S1} is the resistance between the contact and the edge of the channel and R_{S2} is the resistance between the edge of the channel and the metallised gate, as can be see in Figure 26.

R_g = gate resistance

g_{mi} = intrinsic transconductance

The Fukui coefficient (K_F) is normally empirically found and Fukui relates it to material quality and device bias point for the device minimum noise performance.



$$F = 1 + KC_{gs}F2\pi\left[\frac{(RS2+RS1+RC)+Rg}{gm}\right]^{\frac{1}{2}}$$

Figure 26, Schematic of FET channel showing the parasitic resistances.

The Fukui expression can be derived from first principles, by assuming that the noise properties of the transistor can be represented by a noise current generator on the input $\langle ig^2 \rangle$ and a noise voltage generator on the output $\langle e_0 \rangle^2$. The correlation factor C between the two noise generators is assumed to be zero and hence only the thermal noise is considered in the gate circuit. Where $\langle ig^2 \rangle = 4kTG_i\Delta F$, G_i is the equivalent noise input

conductance and is equal to $4\pi^2F^2C_{gs}^2$ $(R_g + R_s)$. Whereas $\langle e_0^2 \rangle = 4kTR_0\Delta F$, R_0 is the equivalent noise output resistance. In Bruncke and Van der Ziel's paper [59] $R_0 = Q/g_{mi}$. Q is the noise parameter and is dependent on material.

Therefore, the Fukui coefficient K_F can be written as $2(\sqrt{Q})^{-1} = 2\sqrt{P}$, where P is the noise factor originally defined by Purcel.

The Fukui equation (3.5.3.6) can be expressed in terms of the material and geometry parameters of the device **[B4]**, and is shown below:

$$NF_{min} = 1 + FK_FL_gv_s^{-1}\{g_{mi}[R_c(n^+, G, \rho) + R_{S1}(n^+, G, D) + R_{S2}(n, G, D)$$

$$+ R_g(G, \rho, F)]\}^{0.5} \qquad (3.5.3.7)$$

L_g is the gate-length and v_s the carrier saturation velocity

R_c = contact resistance as a function of carrier concentration n^+, device geometry G and metal resistivity ρ; R_{S1} and R_{S2} source resistance components as a function of n^+, n, G and surface depletion layer, D; R_g gate resistance as a function of G, F, and gate metal resistivity ρ. The surface depletion layer D reduces the channel area and therefore increases the parasitic source resistance. A schematic showing the relationship of these parameters with reference to the physical layout of the transistor is shown in Figure 8, page 99, **[B4]**.

The Fukui empirical factor K_F was experimentally determined to be of the order of 2.5 for GaAs in agreement with other published result's [60, 57].

A relationship for K_F as a function of material parameters and optimum bias current for short gate-length devices was derived by Delegebeaudeauf [61], and found to give very good agreement with experimental values of K_F for GaAs transistors. The expression for K_F is given below:

$$K_F = 2[I_{opt}/(E_cL_gg_{mi})]^{0.5} \text{ , where } P = I_{opt}/(E_cL_gg_{mi}) \qquad (3.5.3.8)$$

I_{opt} = Optimum current for minimum noise (A).

E_c = Peak velocity field (kV/m).

Equation (3.5.3.8) was substituted into expression (3.5.3.7)

$$NF_{min} = 1 + 4\pi F v_s^{-1}\{(L_g I_{opt}/E_c)[R_C(n^+, G, \rho) + R_{S1}(n^+, G, D) +$$

$$R_{S2}(n, G, D) + R_g(G, \rho, F)]\}^{0.5} \quad (3.5.3.9)$$

Note the saturation velocity (v_s) can be estimated from knowing the f_t (unity gain cut-off frequency) which can be found by the extrapolation of h_{21}.

A computer model was written by the author utilizing the above equation, enabling the optimisation of the transistor parameters, to obtain design information to realize a high frequency and low noise GaAs MESFET. The minimum noise figure was computed as a function of the parameters in equation (3.5.3.9) describing the transistor, these have been published in a number of papers **[B1, B2, B3, B4, B5, B7 and B10].**

It was experimentally found by the author, that the minimum noise figure of the optimised C1 transistor could be further improved, by cooling the device [I7] to the temperature of liquid nitrogen 77K **[B10].** The measured NF_{min} = 0.8dB and the associate gain 9dB at 23GHz, see Figure 27. The improvement was thought to be mainly due to a reduction in the thermal noise and represented one of the lowest recorded NF_{min} for a GaAs MESFET at 23GHz, in 1985.

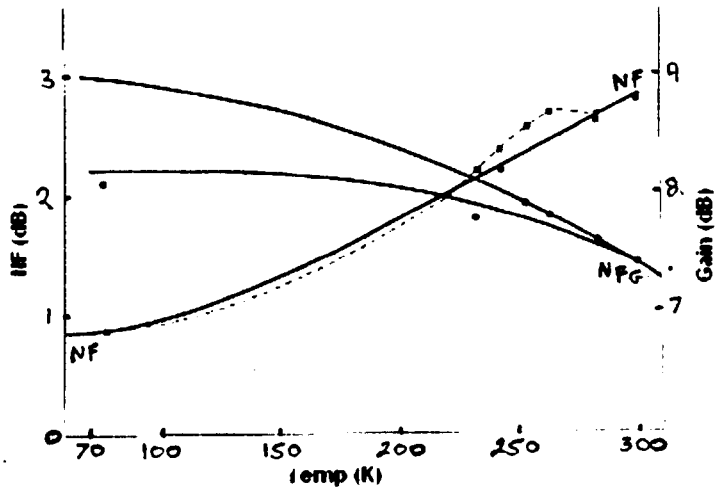


Figure 27: Minimum noise figure at 77°K.

The Fukui analysis has recently been applied, by the author, to the GaN HEMT device, and indicated that a low noise GaN transistor may be feasible **[C1, C3, C4].** This has recently been experimentally verified by a number of international publications [62, 63].

3.6 High frequency measurements

To enable high frequency measurements of the transistor to 40GHz, novel test jigs were developed by the author. Both transistor s-parameters and NF_{min} were measured in K-band (18-26.5GH_z) and Q-band (26.5-40GH_z). As the SMA connector only operated to 18GH_z before multi-moding took place and the 3.5mm air SMA connector was not commercially available, other interface connections between the test-jig and test equipment had to be developed in-house.

Initially, a tapered ridge wave-guide to microstrip launch connection was developed **[I5]** by the author (Figure 5, page 683) **[B6, B7]**, but difficulties were found in obtaining reproducible results, particularly at the higher frequencies 40GH_z. Part of the problem was isolated to the parasitic discontinuity capacitance, created by the gold-tape transition, from the wave-guide tapered ridge to the microstrip line. The position and angle of the gold-tape could vary considerably during assembly, significantly changing the discontinuity parasitic capacitance at the transition **[I6].** To overcome the problem, an E-probe transition was developed by the author, which gave a more reproducible result **[I7].** A figure showing the E-probe test fixture was published in Figure 16, page 102 **[B4].** The disadvantage with the E-probe is the limited –3dB bandwidth, approximately 25%, thus limiting the frequency range over which the transistor could be RF characterised.

The transistor under RF test was mounted in a novel test circuit configuration developed by the author to minimise both the circuit and transistor extrinsic parasitics, for example the source inductance. The test circuit consisted of a well in ridge carrier, which enabled the length of the transistor source bond to be as short as possible, so minimsing the parasitic source inductance. The microstrip circuit was also mounted inside a channel with a 40GHz cut-off frequency, to reduce multi-moding. A schematic drawing and a photograph of the test circuit are shown in Figure 28, and 29 respectively.

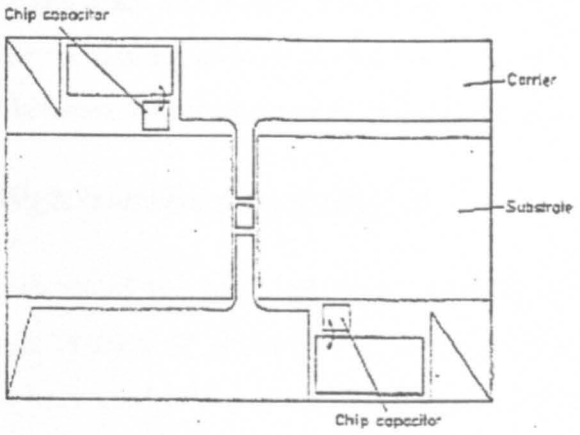


Figure 28: Schematic drawing of the test circuit

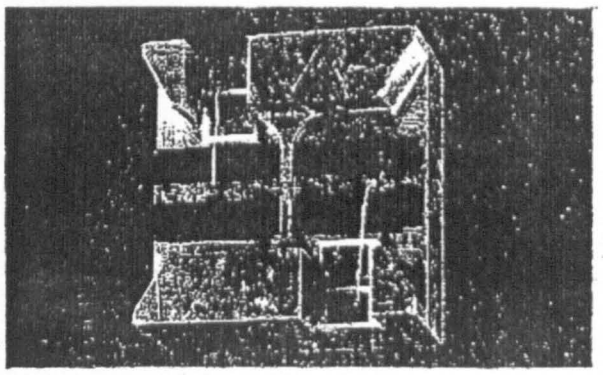


Figure 29: Photograph of the test circuit

To maximise the accuracy of the measurement, the dispersion and RF loss charactersitics of different substrate materials suitable for microstrip substrates were investigated to high frequencies, by the author. The dispersion effects were explored using Itoh Mitra spectral domain analysis [64] and Getsingers semi-empirical approach [65]. Whereas, for the RF losses an analytical approach and D.Meshekar-Syahkal perturbation model [66] were used. The substrate material identified by the author as being most suitable for the application was polished Z-cut quartz, with a substrate thickness of 0.381mm. The results are summarised in the publication **[B6, I5, I20]**.

The gate and drain bias supply was isolated (-40dB) from the RF circuit by a novel low-pass filter, consisting of high-Q chip capacitor and a 1-thou gold diameter wire stitch-bonded between the chip capacitors and the microstrip line, see Figure 29.

4.6.1 High frequency s-parameters

Measurements of the high frequency s-parameters were difficult, as two wave-guide convertors 18-26.5GH$_z$ (HPK52C) WG 20 (WR42) and 26.5-40GH$_z$ (HPR747B) WG 22 (WR28) were used to extend the range of the standard 0.1 -18GHz (HP 8410) network analyzer **[I6,I7,I8,I19,I23]**. [The HP8510 network analyzer is now available to make measurements to 110GHz using a wave -guide connections and up to 60GHz using precision 3.5mm SMA connectors]. The measurements took into account tracking errors, and the calibration utilised a wave-guide load (VSWR = 1.05) and a number of off-set short circuits with different phase lengths. The extended network analyzer system (HP8410) allowed measurements to be made over a 2GHz bandwidth, at any centre frequency within the bandwidth of the convertor, this was primarily due to having to set the frequency manually. Never-the-less, useful high-frequency s-parameter data was obtained, which was directly compared with the extrapolated s-parameter data from the lumped and distributed electrical equivalent circuit models. Figures 30, 31 and 32 show the measured s-parameters s11, s22 and s21 to 23.0GHz as a comparison with the extrapolated data for both the lumped and distributed equivalent circuit models.

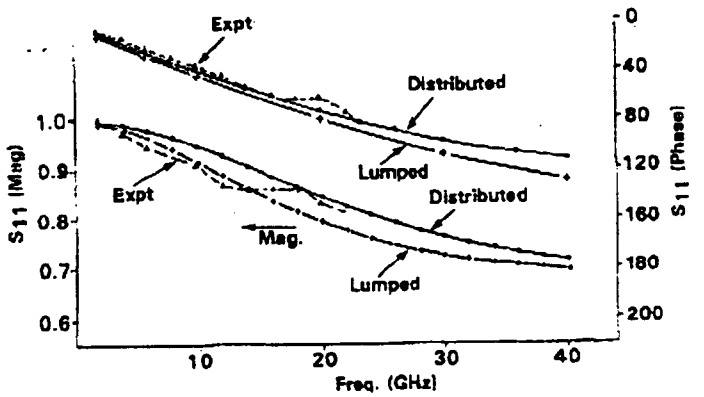


Figure 30: s11 measured and modelled

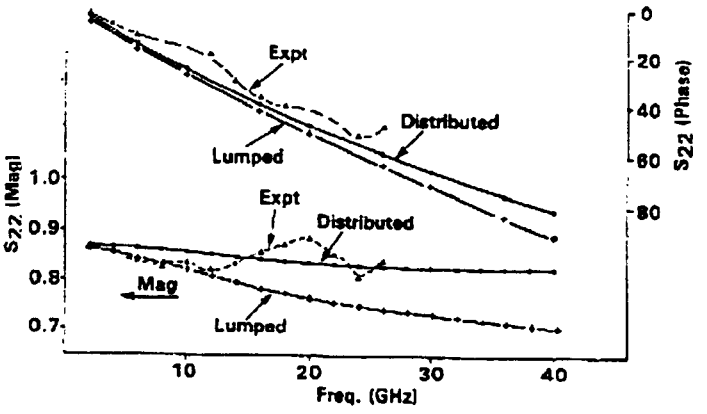


Figure 31: s22 measured and modelled

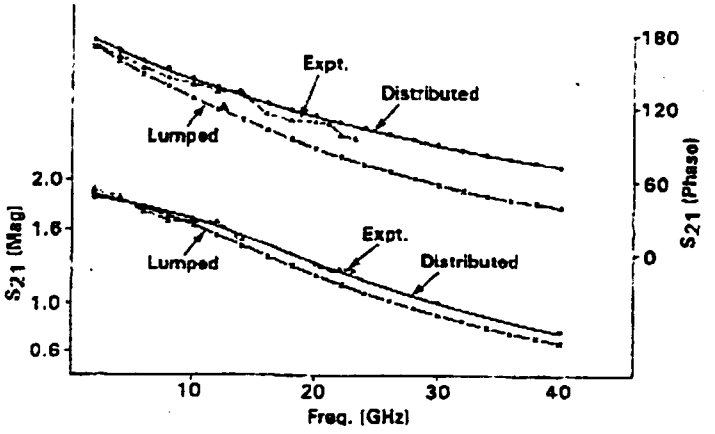


Figure 32: s21 measured and modelled

3.6.2 High frequency gain and minimum noise measurements.

Initially, the high-frequency gain and NF_{min} measurements were made by the author tuning the device by moving precision laser cut slivers of metal on the 50-Ohm microstrip line. This method allowed a satisfactory maximum available gain (MAG) measurement to be obtained, following a $1/(freq)^2$ dependence. However, with increasing frequency the measured minimum noise-figure was found to be much higher than predicted by the Fukui noise theory. It was thought that the tuning slivers provided a large radiation discontinuity at the high-frequencies leading to significantly higher levels of microwave losses, and consequently a higher than expected NF_{min}. An alternative

method was developed by the author, leading to a reduced number of tuning slivers and therefore circuit RF losses, enabling a more accurate NF_{min} measurement.

It was experimentally found that significant improvements in the measurement technique were obtained by using the measured small signal s-parameter at the low noise bias point, to design a matching circuit at the characterisation frequency, for example $23GH_z$ and $32GH_z$. Only a small amount of extra tuning, using the metal slivers, was required to optimize the match, resulting in lower radiation losses, enabling improved measurement accuracy to both the gain and NF_{min}. The improvement in the gain at 23GHz is pictorially shown in Figure 33.

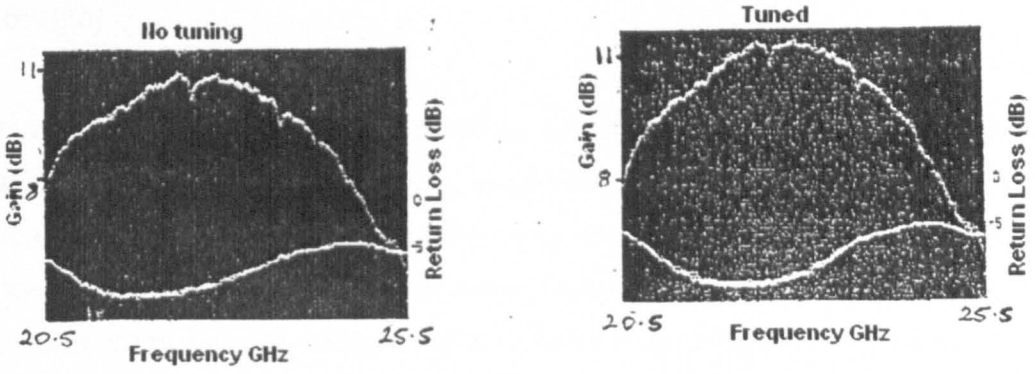


Figure 33: Fine tuning using metal slivers

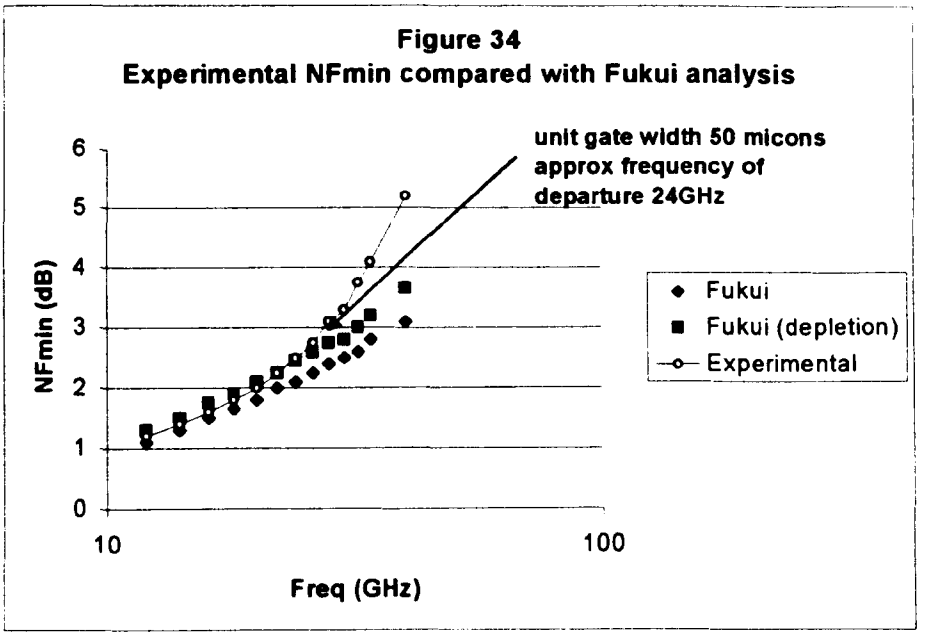
The described method was feasible, as a separate set of measurements showed that the optimum input impedance (Z_{opt}) for minimum noise figure at $14GH_z$, was close in magnitude and phase to the impedance derived from small signal s-parameters at low noise bias. Secondly, the selected devices for high-frequency characterization at low noise bias condition showed consistent s-parameters measurements over identical frequency-range. The assumption was made that Z_{opt} and the impedance derived from the small signal s-parameters at low noise bias would be similar in magnitude and phase at high frequencies. Therefore, the small-signal equivalent circuit model developed at the low noise bias condition could be used to extrapolate the s-parameter to the high frequencies and the resulting impedance would be similar to Z_{opt} for minimum noise figure. A matching-circuit was designed using the high frequency s-parameter measurements at the low noise bias condition, and then used to measure the NF_{min} of the transistor. Hence, only a small amount of circuit optimisation by tuning with the external

metal slivers was required for the minimum noise figure measurement. This approach was adopted for all the high-frequency characterization measurements.

The NF_{min} of transistors with different unit gate-widths were measured as a function of frequency and published in **[B2, B3, B4].** It was experimentally found that the optimum drain current I_{ds} for minimum noise operation, was 15 to 20% of $I_{ds.}$ and was similar to other published work [68]. Therefore, in the Fukui expression I_{opt} was calculated as ≈ 20% of the I_{dss}. Recent work on AlGaN/GaN HEMT devices has also indicated a similar ratio [69]. Although some workers using GaN devices have reported a lower ratio I_{opt}/I_{dss} = 10% [70].

The author found that the measured NF_{min} for different unit gate-widths obeyed the classical linear increase with frequency, as predicted by the Fukui expression (3.5.3.9) to a break frequency (f_B). Beyond this frequency, the NF_{min} increased more rapidly with frequency than predicted by the Fukui model; further, the break frequency appeared to be dependent on the unit gate-width (w) of the transistor, as illustrated in Figure 34.

Figure 34
Experimental NFmin compared with Fukui analysis



Beyond the break frequency (f_B), the experimentally observed rapid increase in NF_{min} **[B3]** with frequency, could not be accounted for by either the skin-effect in the gate resistance R_g or by including the higher order terms in the Fukui analysis [57].

The Fukui transistor noise model is lumped element and although adequate at low frequencies; at the higher frequencies the transistor geometry may start to behave as a distributed network due to cross-coupling between the different electrodes of the structure. According to Hirachi [71] the general criterion for describing the point at which a passive element can be modelled as a distributed rather than a lumped component occurs when the dimension of the component approaches approximately $\lambda_g/20$, where λ_g is the guided wavelength.

The distributed model was used to determine the normal propagation modes and associated velocities for the geometry of the C1 transistor structure shown in Figure 35.

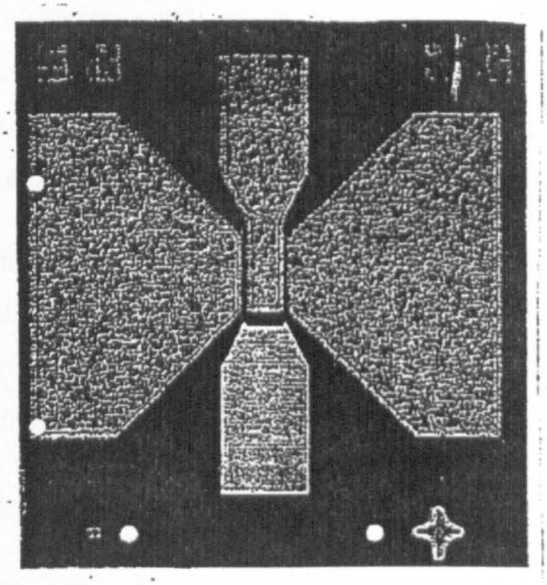


Figure 35: C1 transistor structure

An average of the dominant velocities was simulated and the average λ_g calculated, for each unit gate-width at the break-frequency. These results are given in the table 4 below:

Table 4

Unite-gate width	Frequency of departure	Slow wave	Fast wave	Average
100 microns	14GHz	$\lambda_g/7.2$	$\lambda_g/36$	$\lambda_g/21$
65 microns	20GHz	$\lambda_g/8.0$	$\lambda_g/38$	$\lambda_g/23$
50 microns	26GHz	$\lambda_g/8.0$	$\lambda_g/38$	$\lambda_g/23$
35 microns	34GHz	$\lambda_g/8.0$	$\lambda_g/40$	$\lambda_g/24$

The experimental results indicated that the change from a lumped to distributed model occurred at approximately $\lambda_g/20$, the value defined by Hirachi, which also appeared to be at the frequency the NF_{min} departed from the Fukui model. This frequency was defined as the break-frequency $f_B(w)$, and is dependent on the unit gate-width (w).

This led to a modification to the Fukui equation (3.6.2.1), which is fully described in Ref **[B3].**

In the limit when $f >> f_B(w)$ and $C_1 << C_0$, then distributed effects need to be taken into account and the minimum noise figure NF_{min} can be written as:

$$NF_{min} = 1 + C_0 f + 0.23 C_1 C_0 f^2 \quad + \text{higher order terms} \qquad (3.6.2.1)$$

When the frequency is less than $f_B(w)$, distributed effects are not taken into account:

$$NF_{min} = 1 + C_0 f \text{ (standard Fukui equation)} \qquad (3.6.2.2)$$

Where $C_0 = 4\pi v_s^{-1}\{(L_g I_{opt}/E_c)[R_c(n^+, G, \rho) + R_{S1}(n^+, G, D) + R_{S2}(n, G, D) + R_g(G, \rho, f)]\}^{0.5}$ (3.6.2.3)

The coefficient C_1 was an empirically derived coefficient and was found to be 0.088 for GaAs MESFET. At frequencies where the simple Fukui lumped element model was still valid, $C_1 = 0$. The physical interpretation of C_1 may be related to a cross-coupling factor between the drain and gate noise sources. When cross coupling between electrical elements starts to become significant for example the gate drain capacitance C_{gd}, then it is no-longer valid to assume zero cross-coupling between the drain and gate noise sources.

The expression (3.6.2.1) gave good agreement with experimental results **[B3],** but was limited in use as the coefficient C_1 had being empirically derived for the **C1** transistor. However, it did enable further optimisation of the C1 transistor structure for low noise operation resulting in a proposed structure shown in Figure 36, which was subsequently known as the C3 low noise MESFET.

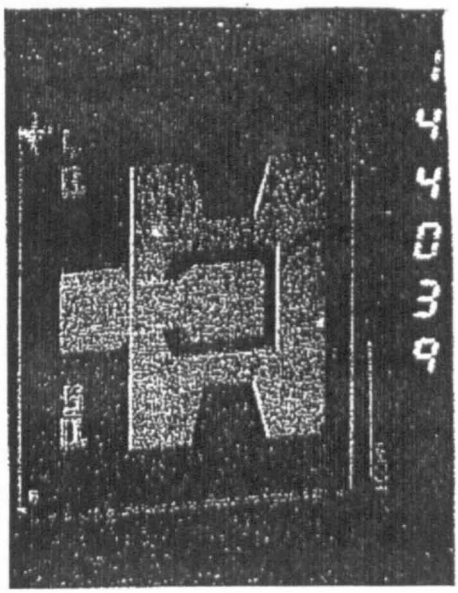


Figure 36: The C3 GaAs MESFET

Cappy [74] included cross-coupling between the gate $\langle ig^2 \rangle$ and drain noise $\langle id^2 \rangle$ sources in a lumped element model and showed that:

$$\langle id^2 \rangle = \{4kT\Delta F g_m L_g A / C_{gs}\} B \qquad (3.6.2.4)$$

where $A = f(\alpha Z + \beta I_{ds})$ and $B = 1 + \omega^2 C_{gd}^2 / g_d^2$

C_{gd} the gate drain capacitance, g_{ds} the output conductance, and I_{ds} the drain source current where β and α are fitting factors. At low frequencies and with a small C_{gd}, $\langle id^2 \rangle$ is not dependent on frequency whereas at high frequencies and a high C_{gd}, $\langle id^2 \rangle$ is dependent on frequency. The frequency at which the noise became dependent on the cross-coupling between the gate and drain was defined by Cappy as $f_0 = g_{ds}/2\pi C_{gd}$. The frequency f_0 does not appear to be depended on the unit gate-width as both g_{ds} and C_{gd} are functions per mm of total gate width.

It should be noted that the equivalent Fukui coefficient can be written as $K_F = \{L_g A / C_{gs}\}^{0.5} B^{0.5}$.

Therefore, the minimum noise figure NF_{min} can be calculated and was found to be dependent on the magnitude of the gate drain capacitance C_{gd} and drain source conductance g_{ds}. In physical terms the magnitudes of C_{gd}/mm and g_{ds}/mm will determine the frequency at which the gate drain noise cross-coupling can no-longer be neglected. Using the Cappy work the minimum noise figure NF_{min} can be written in the form shown below:

$$NF_{min} = 1 + Cxf[1 + (f/f_0)^2]^{0.5} \qquad (3.6.2.5)$$

Where $C_x = 4\pi \{L_g A C_{gs} / g_{mi}\}^{0.5} \{[R_c(n^+, G, \rho) + R_{S1}(n^+, G, D) + R_{S2}(n, G, D) + R_g(G, \rho, f)]\}^{0.5}$

In the limit when f is very large both equations 3.6.2.1 and 3.6.2.5 converge to the form

$NF_{min} = 1 + Af^2$, where A is a coefficient.

Both approaches indicate that the minimum noise figure increases at a faster rate with frequency when cross-coupling via the feedback elements between the drain and gate electrodes become significant. The Cappy approach suggests that the cross-coupling is totally dependent on the channel geometry which will determine C_{gd} while the material

properties will have a more significant on g_{ds}, thus the frequency at which cross-coupling occurs is independent of the unit gate width and number of gate electrodes. However, the experimental work presented suggests that NF_{min} is dependent on the unit gate-width, and the point at which NF_{min} departs from the classical Fukui theory coincides with the frequency when the width of the structure is approximately $\lambda_g/20$. This electrical length has been defined [71] as the point when a structure should be considered as a distributed rather than a lumped network.

Further research work is required to be carried out in order to determine the significance of the unit gate-width on the noise performance of the transistor. For example, consider an FET operating in the saturation region beyond the knee point, then $g_{ds} \approx 2\varepsilon'\varepsilon_0 W v_{satbuffer}/kL_{eff}$ and $C_{dg} \approx L_{eff}W\varepsilon\varepsilon_0/\alpha$ [72]. Where W = total active width of the transistor, ε' = relative dielectric constant of the buffer layer, ε = relative dielectric constant of the active layer, $v_{satbuffer}$ = carrier saturation velocity in the buffer layer, and α the depletion width. The term k is a factor relating the effective gate-length (L_{eff}) to the thickness of the buffer layer, and for GaAs $k \approx 1/3$. The above assumption was made on the basis that the total width of the transistor was active. If, however, the width of the transistor was a single-stripe and its length increased, the resistive contribution increases and at a predetermined frequency only part of the width would be active [42, 72], therefore the 'effective' depletion layer depth α would decrease. This would result in reducing K and therefore f_0. Hence, transistors of the same gate length but with a larger unit gate-width (w_{unit}) would have a lower f_0, see equation (3.6.2.6) which has been experimentally observed **[B2].**

$$f_0 \approx v_{satbuffer}K\varepsilon'/(\pi\varepsilon L_{eff}^2) \text{ and } K(w_{unit}) = \alpha/k \qquad (3.6.2.6)$$

To a first approximation f_0 can be increased, by reducing the gate-length and the unit gate width when assuming the carriers have reached saturation in the buffer region. The simple argument suggests that the approach published by Cappy is also dependent on the unit gate-width.

Note short unit gate-widths will also reduce the parasitic gate resistance, and therefore the thermal noise contribution.

3.7 Conclusions

The described GaAs MESFET devices were designed and fabricated during 1980-1986 giving a European state-of-the-art performance. The transistors were successfully used in a number of applications which included 23 and 32GH_z satellite-up and down-links **[B4]** and a 30GH_z high-gain low-noise amplifier for ESA [73]. A comparison of NF_{min} with frequency for state-of-the-art GaAs MESFET and HEMT performance in 1985 is summarised in Figure 37.

The characterisation techniques developed are still widely used, albeit improved de-embedding models have been developed, which have superceded the simple de-embedding procedure using the unilateral model of the FET.

The Fukui Noise model is still widely used as it offers many benefits, including a first order approximation of the minimum noise figure of the transistor, particularly if the work of Delagebeaudeuf [61] is included to estimate the Fukui Coefficient (K_f) from the material parameters. With the increased understanding of the electrical and physical mechanisms within a transistor, which included the mutual coupling effects at higher frequencies the description of the device was improved. The distributed effects operating within a transistor have not been fully addressed and many high frequency models still rely on the lumped element approach. This has possibly been driven by the improved capability of s-parameter measurements to very high frequencies i.e. 110 GH_z, eliminating in most applications the requirement to extrapolate to high frequencies from a low frequency transistor equivalent model.

INDUSTRIAL REFERENCES supporting the work I5, I6, I7, I8, I19 ,I20, I21 and I23.

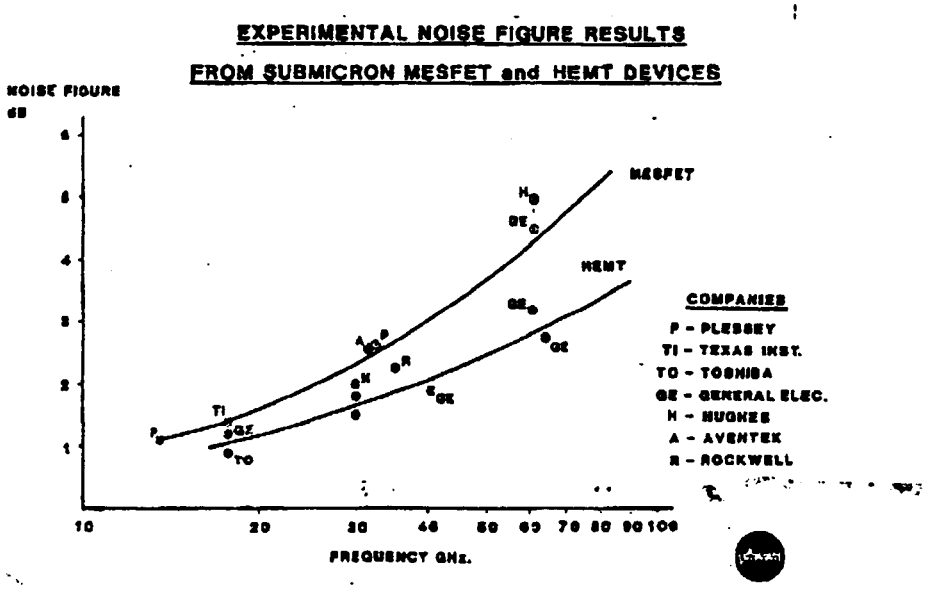


Figure 37: Comparison of GaAs MESFET NF_{min} in 1985

CHAPTER 4: TRAVELLING WAVE STRUCTURES

4.1) Introduction

An ideal transmission line with a periodic (Δx) capacitive (ΔC) and inductive (ΔL) elements and correctly terminated, will theoretically have a bandwidth $\Delta f = (1/\Delta x 2\pi[\Delta L \Delta C]^{0.5})$ GH_z. The picture can be extended further by assuming the periodic elements also include an active gain block, thereby realising an amplifier with a bandwidth (Δf) and a gain directly proportional to the length of the transmission line. In reality, a real transmission line will contain loss elements, which will degrade the magnitude of the ideal gain.

The high-frequency performance of a FET is limited to a first order of approximation by the magnitude of its input capacitance C_{gs} i.e. $f_t = g_m/\{2\pi(C_{gs})\}$. If the input capacitance C_{gs} and the gain element g_m of the FET are combined as periodic elements within a transmission line, then a large number of elementary FETs could be connected in parallel to increase the gain. Further, as each element would be sequentially fed the limitation in bandwidth due to high input impedance, would be avoided. The above concept of travelling wave operation was first published in 1948 [74]. Recent publications have shown the feasibility of realizing extremely wide bandwidths, with a reported monolithic capacitive coupled travelling wave amplifier (TWA) having a 340 GH_z gain- bandwidth product, using 0.15 micron gate-length InGaAs/InAlAs HEMTs [75].

A number of publications on FET travelling wave amplifiers have appeared in the open literature between 1969 and the early 1980's, and two are cited here [76, 77], and report on discrete transistors mounted in a periodic network. The work to be now described in this thesis was believed to be the first published experimental measurements on a 'true' travelling wave transistor (TWF) **[B12].** It consisted of a transistor with a continuous 1-micron gate, which supported a traveling-wave along its active width W (3mm), the velocities of the traveling-waves along the gate and drain electrodes were balanced by periodically positioned drain/source overlay capacitors. The parasitic resistance of the gate R_g was reduced by using a metallised 'T' profile gate structure. The research/design

work carried out in the demonstration of the TWF led directly to the development of a new transistor known as the LINEAR GATE TRANSISTOR (LGT) **[B9]**, this device was a subject of a national and international patent **GB2156152 (Appendix 5).**

4.2.1) Operation of Travelling Wave Structures

There are two forms of travelling wave structures the most common is the travelling wave amplifier (TWA) and the second form is the travelling wave FET (TWF).

The TWA consists of discrete FET devices connected in parallel using a hybrid or monolithic circuit technology as shown in figure 38.

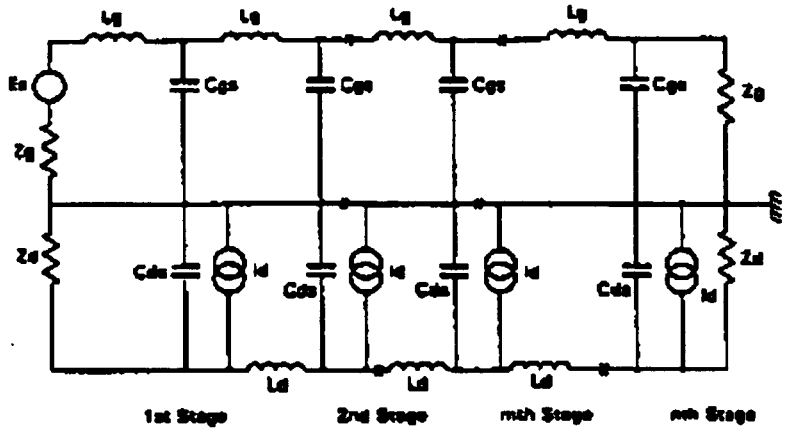


Figure 38 Travelling Wave Amplifier

The input signal is fed into the electrode connected to the gates of the transistors and the amplified signal is extracted from the drain electrode. To obtain gain from the travelling wave amplifier the phase between the gate electrode and drain electrode has to be maintained along the length of the TWA. To a first approximation the phase velocity of the gate wave is given by $\frac{\Delta l_g}{\sqrt{L_g(C_g + \frac{C_{gs}}{\Delta l_g})}}$ and the phase velocity of the drain wave is

given by $\frac{\Delta l_d}{\sqrt{L_d(C_d + \frac{C_{ds}}{\Delta l_d})}}$ where Δl_g and Δl_d are the periodic lengths of the gate and drain electrodes and L_d, L_g, C_d and C_g are the inductances and capacitances per unit length of the gate and drain transmission lines respectively. While C_{gs} and C_{ds} are the FET gate source and drain source capacitance per unit length. Normally in an FET $C_{gs} > C_{ds}$ and therefore the phase velocities will not be identical. In the TWA the inductance of the drain electrode is increased by meandering the drain electrode ($\Delta l_d >> \Delta l_g$) making the phase velocity on the gate and drain electrodes identical

$$\frac{\Delta l_g}{\sqrt{L_g(C_g + \frac{C_{gs}}{\Delta l_g})}} = \frac{\Delta l_d}{\sqrt{L_d(C_d + \frac{C_{ds}}{\Delta l_d})}}.$$

The signal on the gate electrode will continue to drive the signal on the drain electrode in phase, resulting in 'active transmission line'. As the transmission line electrodes are lossy the input-signal exponentially decays as it travels down the gate electrode and at some point will no-longer have sufficient amplitude to drive the signal on the drain electrode. Work by Ayasli [78, 82] has shown that the maximum number FET stages is approximately 7. After which the gain will start to decrease.

Ayasli showed that the gain of the TWA is given by $G = g_m^2 n^2 Z_d Z_g / 4$ where $Z_d = (\frac{L_d}{(C_d + \frac{C_{ds}}{\Delta l_d})})^{0.5}$ and $Z_g = (\frac{L_g}{(C_g + \frac{C_{gs}}{\Delta l_g})})^{0.5}$ are the characteristic impedance of the drain and gate electrodes respectively. It can be seen, by meandering the gate electrode the inductance is increased resulting in a high Z_d, thereby increasing the overall gain of the TWA.

The competing device to the TWA is the traveling wave FET (TWF) in which the gate, drain and source electrodes are parallel with one another and the FET structure is

periodically built into the transmission line, see Figure 39. The transmission line is designed to increase the inductive coupling between gate and drain electrodes, which is feasible within this geometry. The phase velocities of the waves travelling along the drain and gate electrodes are equallised by increasing the drain-source capacitance C_{ds} using overlay capacitors Figure 39. The input signal traveling along the gate electrode drives the output signal on the drain electrode, but this time because of the inductive coupling some of the signal on the drain line drives the input signal on the gate electrode so sustaining the input signal as it travels along the lossey gate electrode. Therefore, in principle, the gain of the TWF can be increased simply by increasing its length unlike the TWA.

However, it should be noted that as overlay capacitors are used to equallise the phase velocity on the gate and drain electrodes Z_d is reduced this time, unlike the TWA, therefore the gain of the TWF is lower than that of the TWA for a comparable active transmission line length.

4.2.2) Travelling Wave FET (TWF)

The described prototype travelling wave FET (TWF) was designed by H. D. Rees of R.S.R.E., Malvern and engineered into a working transistor at the Allen Clark Research Centre. This work entailed an extension of the Rees' theory in the form of design software **[B12].** The mathematical model of the TWF and the subsequent development of the design software largely carried out by A. Holden **[B12, B13, B14].** The microwave design and realization was carried out by the author **[B12, B13, B14]** and the formidable task of fabricating the low resistance continuous 3mm wide gate of 1 micron gate length, by D. Daniels **[B12].** The following section outlines the computer model for information only.

4.3) Computer model

The computer model was developed by A. Holden in discussion with the author who provided the transistor equivalent circuit model and microwave circuit characteristics. The model calculated the 'infinite line' eigenmodes and output characteristics (s-

parameters and gain) for a transistor with a given electrode spacing geometry, intrinsic parameters, width (W), and impedance boundary conditions. All of the geometrical capacitive and inductive parameters due to the external transmission line electrodes (source, gate, drain) were calculated from first principles.

The model was based on the quasi TEM transmission line theory and considered the case of three-coupled transmission lines (source, gate and drain electrodes). Coupling between the electrodes was considered to occur via the geometrical capacitance and inductance elements and the elements within the intrinsic FET. A.Podgorshi [78] and Ayasli [79] only considered the example of two transmission lines coupled by the transconductance g_{mi} of the FET.

As the intrinsic FET was incorporated through an equivalent circuit the field analysis was limited to the quasi TEM approximation. This has recently been re-calculated using a full-field analysis by Farina and Rozzi [80]. The quasi TEM analysis presented was reduced to calculating the properties of an electrical circuit with distributed components, and could be broken into 3 parts:

1) ***The geometrical layout:*** The geometrical arrangement adopted for the travelling wave FET is shown in Figure 39, and the active part of the structure (intrinsic FET) was where the source/gate/drain electrodes were closest together. The three electrodes were positioned on the front-face of a dielectric slab, which was mounted on a metallised ground plane. The mutual capacitance and inductance elements were calculated for the structure.

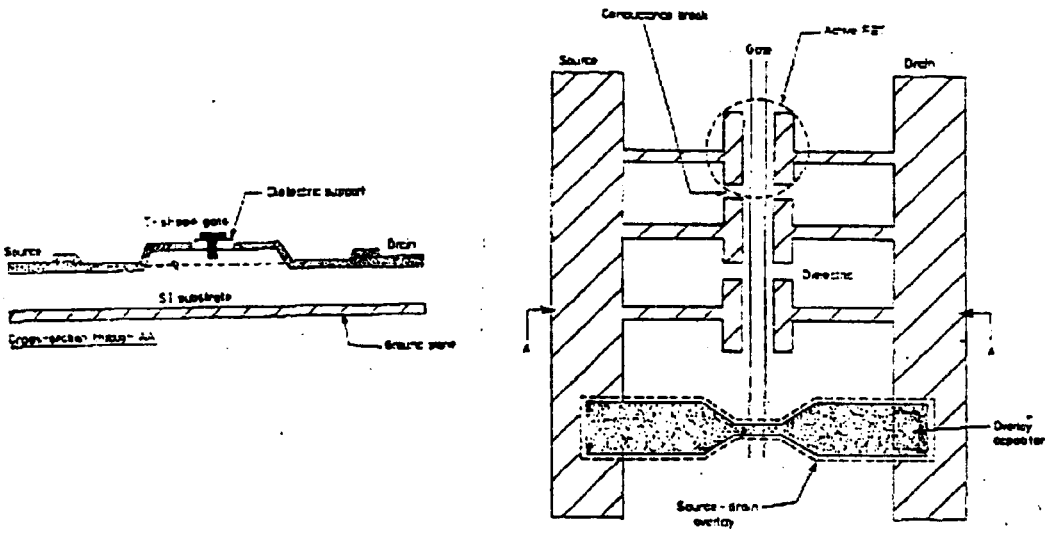


Figure 39 Geometrical structure of the TWF

2) ***The intrinsic FET:*** The active FET components were assumed to be periodically distributed along the width of the device. The intrinsic FET model followed the earlier work developed by the author and described in section (3.5).

3) ***To phase balance gate and drain transmission waves:*** The geometry included the addition of overlay capacitors between the source and the drain electrodes, in order to balance the larger source-gate depletion capacitance and thereby maintain the same phase between the travelling wave on the gate and drain transmission lines.

It is interesting to note that there are at least three possible forward modes of propagation, excluding the backward (reflected) waves. Only one of the modes showed growing gain, the other two modes were lossey.

A full description of the computer model was published in **[B14].**

4.4) Design of Travelling Wave FET (TWF)

The balancing of the travelling waves on the gate and drain electrodes is very important and was achieved by lumped overlay capacitors on the drain line with earth contacts bridged to the source electrode, as shown in (Figure 1a and b, page 62, **[B12]**).

The key to TWF operation was the growing-wave mode, which could be activated when the gate and drain electrodes were arranged to maximise their inductive coupling and the phase velocities of the travelling waves on the gate and drain electrodes were matched.

To launch and receive the growing-wave, balun input and output circuits were designed by the author and fabricated on microstrip **[B12, I9, I10]**. The design was subject of a patent application. In this configuration, the appropriate voltage phases (0^0 on the gate and 180^0 on the drain) were required to excite the growing-wave Figure 40. The designed and fabricated balun circuits were found to have a high RF loss, which significantly degraded the performance of the TWF. It was also experimentally found that the TWF device was reciprocal $S_{21} = S_{12}$ and therefore provided no isolation between the input and output terminals. Hence, the TWF required ***perfect matching over the bandwidth*** to prevent internal reflections and standing waves being set-up **[B12]**.

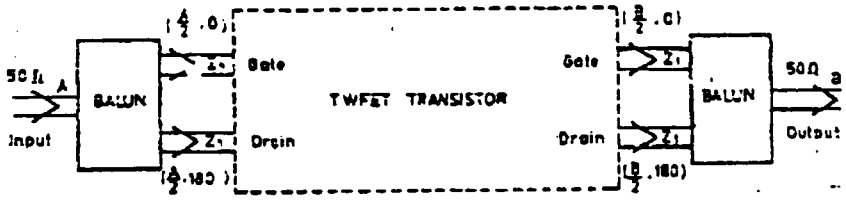


Figure 40 Schematic showing the feed and output circuit for TWF.

The growing-wave is a result of the feedback of power from the drain line to the gate line and provided the phases of the waves are identical the signal on the gate line is increased. In this way the gate continues to drive the active transistor as the wave passes across the

width (W) of the device and the output signal power increase exponentially. Hence, the gain of the TWF increases with increasing transistor width (W) without limit. However, a limit is automatically imposed by the requirement of having to match the growing-wave at each end of the device. The characteristic impedance of the mode was found to be around 20 Ohm and any mismatch at the output is reflected back along the structure. As the device was reciprocal the reverse wave also grows on its return and a very strong 'Fabry-Perot' type of resonance is set-up. Figure 41 shows the TWF matched to 20 Ohms, the theoretical plot indicates a perfectly flat bandwidth as the matching circuits were assumed be ideal, whereas the experimental plot shows a strong Fabry-Perot resonance.

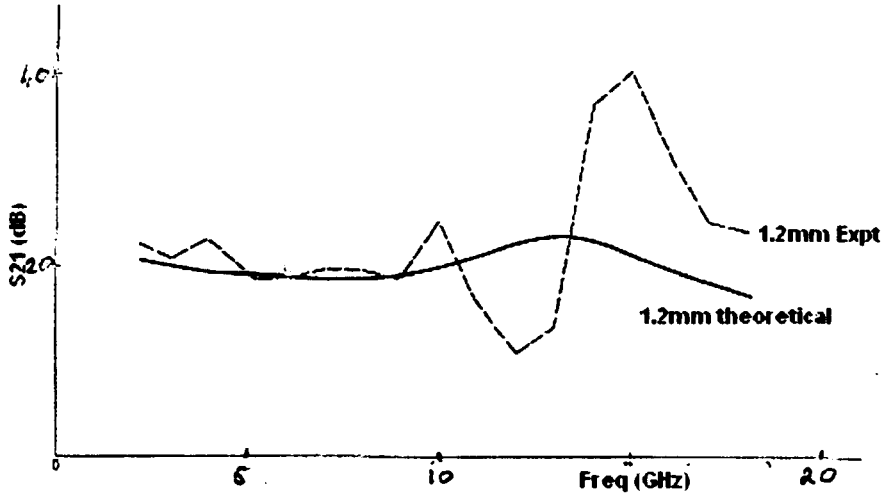


Figure 41 TWF fed using a 20 Ohm balun circuit

Further, if the same device was then matched to 50Ohms, a mis-match would be generated which is theoretically predicted in Figure 42, along with the comparable experimental plot. The figures 41 and 42 show that the larger the degree of mis-match the larger the resonance. The author believes this was the first time a growing-wave has been experimentally observed, along with the Fabry Perot resonance in a TWF. To improve the RF isolation, the TWF was single-end fed and the respective gate and drain idle electrodes were terminated by the characteristic impedance. The theoretical and experimental gain performance was very much reduced with frequency **[I10].**

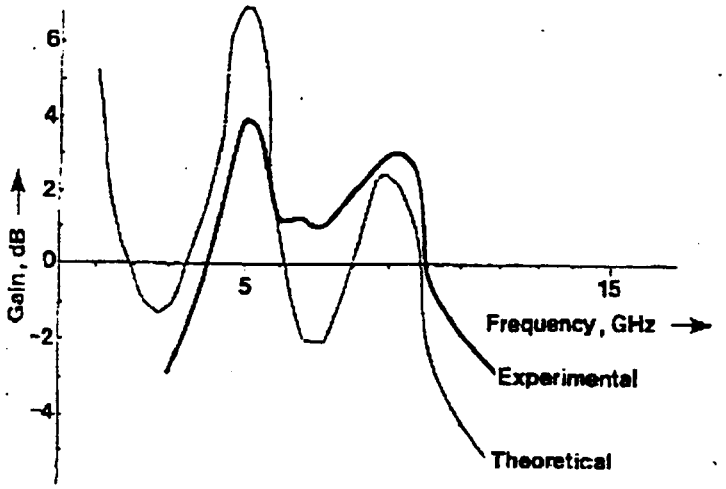


Figure 42 TWF fed using a 50 Ohm balun circuit

The above was seen as a fundamental problem with the experimental TWF. To obtain sufficient gain, devices between 7 and 10mm of continuous active width would be required and the computer analysis and experimental results showed that ***any mismatch*** would cause very strong 'Fabry Perot' resonance thereby destroying the wide-bandwidth with a flat-frequency response.

4.5) The linear gate transistor (LGT)

The travelling wave amplifier (TWA) uses discrete devices **[B13]**, and does not exhibit evidence of a growing-wave consequently there is an upper limit to the number of active devices which can be used. This is due to the increasing loss in the gate line thereby attenuating the input signal to each subsequent transistor. The maximum number of gain stages has been experimentally and theoretically shown to be between 5 and 7 devices [81]. However, the TWA has a higher characteristic impedance ($Z_0 = [L/C]^{0.5}$) than the TWF, as the balancing of the gate and drain waves is normally accomplished by meandering the drain electrode (amounting to increasing the inductive loading) rather than capacitive loading used in the TWF. The input signal to the TWA is fed to the gate and the output is taken from the drain, therefore there is no requirement to match the growing-wave. The TWA also has good RF isolation between the input and output ports.

The TWA can be connected directly to a 50-Ohm feed without the complex balun circuit and will provide 9dB of gain [82], whereas a TWF with a similar active width (W) theoretically will only provide 4dB of gain.

The above understanding enabled a new device to be developed, which incorporated the merits of both TWA and TWF. By maintaining a linear gate-line as in the TWF, adopting the meandered drain-line from the TWA and arranging for the drain to couple closely with the gate within separate but integrated active FET regions, a TWA with high drain-gate feedback was created and called the **linear gate transistor (LGT).** A schematic of the LGT is shown in Figure 43.

This LGT was modelled using the developed software and shown to support a growing-wave, provided the gate-length was less than 0.6 micron and had a very low RF resistance, necessitating a metallised 'T' profile gate structure. The modelled LGT device was shown to have conventional gain at low frequencies, comparable to the TWA, but would support a growing-wave. Thus, giving the advantage that the number of active sections in the LGT was not limited, thereby providing the potential of high gain and wide-bandwidth see Figure 10, page 94 **[B13]**.

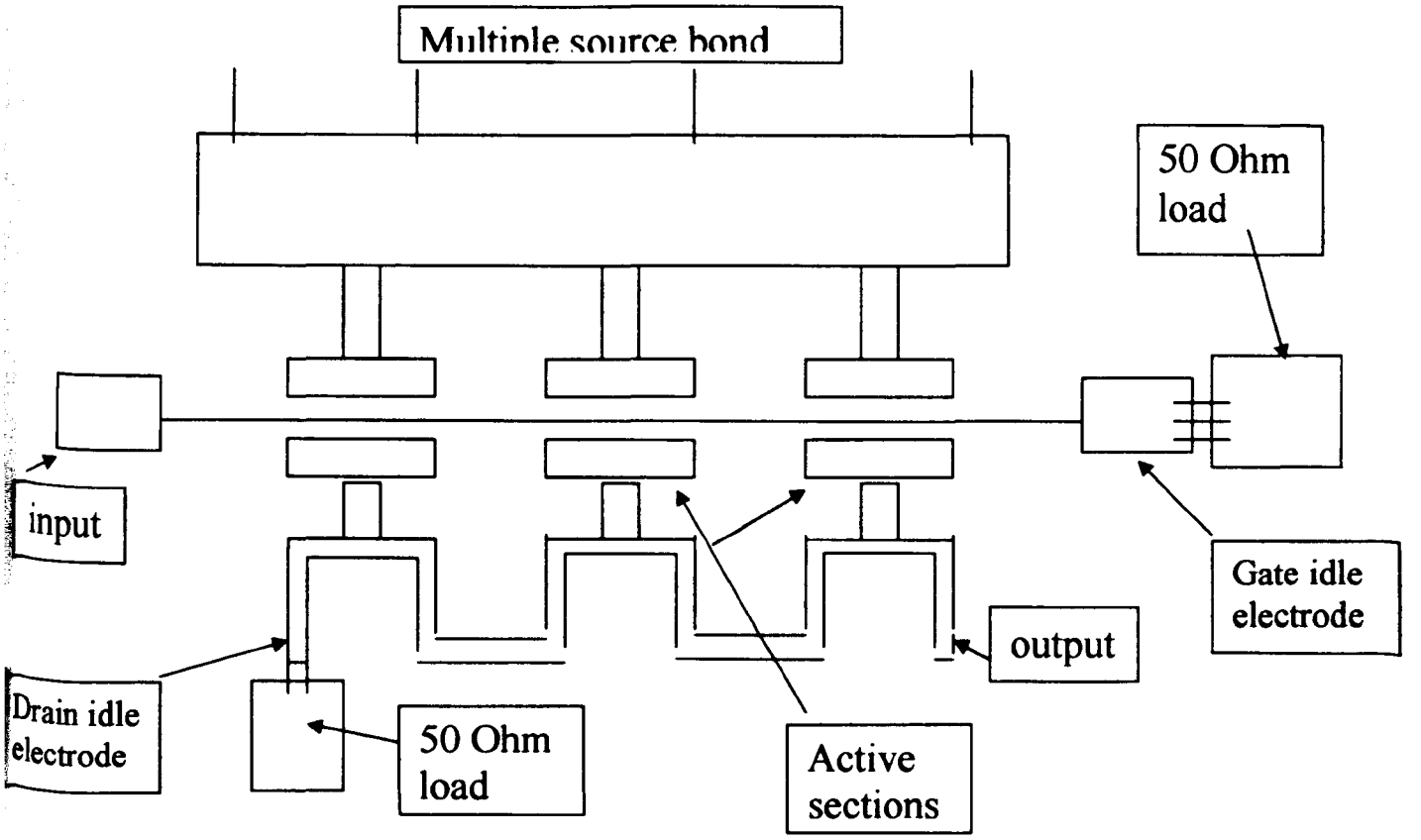


Figure 43, Showing schematic layout of the LGT with a characteristic impedance of 50Ohms

A prototype device with a total width of 2mm was fabricated and a photograph of the transistor is shown in (Figure 9, page **[B13]**).

There were a number of problems regarding the fabrication, the main difficulty, the realisation of a gate-length of less than 0.6 microns over a continuous length of 2.0mm and having a very low RF resistance (see section 4.3.1). This was achieved by fabricating a 0.5 micron gate-length using standard photolithography and evaporation, and then forming the 'T' profile by a subsequent sputtering process to a total thickness of 1.5 microns. The measured dc resistance of the gate stripe was 6 Ohm/mm, giving an estimated RF resistance of 2 Ohm/mm. The transistor exhibited good pinch-off characteristics and an extrinsic transconductance (g_{mc}) of approximately 70mS/mm. The extrinsic transconductance was much lower than for a conventional 0.6 micron gate-

length MESFET (180mS/mm), suggesting that the parasitic source resistance (R_S) was high. This may have been the result of a relatively thin metallised gold source and drain electrodes resulting in a high contact resistance (R_c), and a wide source gate spacing to accommodate the gate 'T' profile. Future devices will require these electrodes to be gold plated to around 2-5 microns, and the geometry to be re-optimised. The typical drain gate breakdown voltage, VB_{DG} and saturation current I_{sat} were 17Volts and 0.6A respectively.

4.5.1) RF characterisation

The LGT was RF characterised by mounting it in a 50-Ohm test-fixture without impedance terminations to the gate and drain idle electrodes, see the schematic of the LGT in Figure 43. Figure 44 shows the experimentally measured S_{21} without any external tuning, which gave good agreement with the computer model. The degree of ripple across the bandwidth was directly related to the impedance match provided by the terminations.

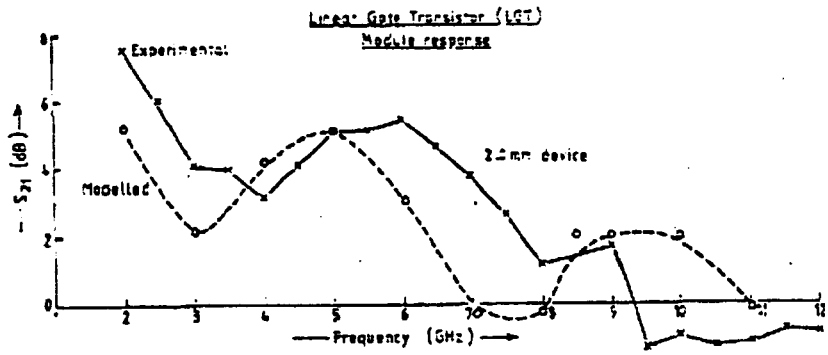


Figure 44,

Comparison between experiment and computer model, without terminations

To estimate the magnitude of the gain ripple (S_{21}) with respect to the device match, the device was simulated with and without terminations as shown in Figure 45 and Figure 46.

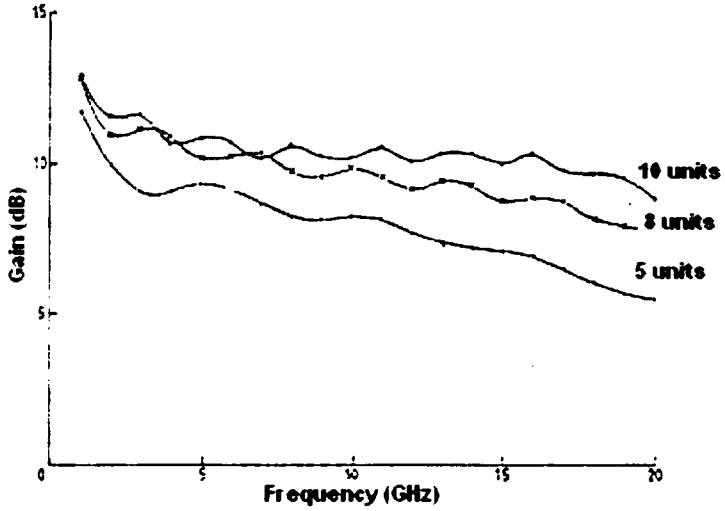


Figure 45

Simulation of s21 with terminations on the 'idle' ports

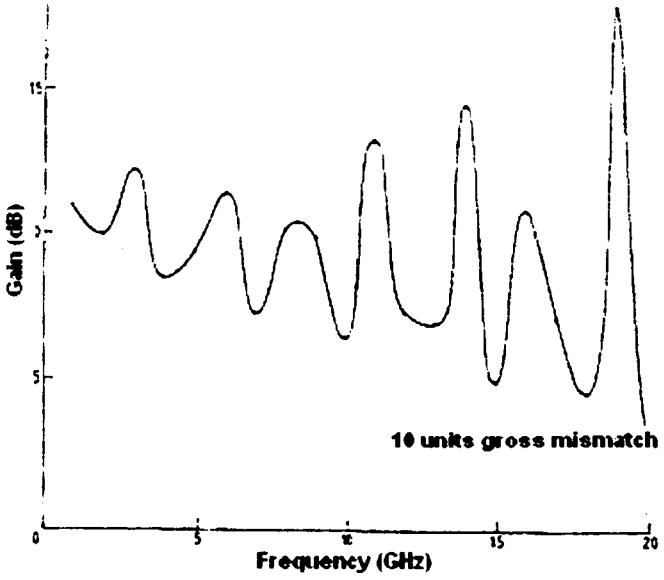


Figure 46

Simulations without terminations to the 'idle' ports

The input and output port return losses were of the order of –10dB across the measured bandwidth, and the reverse isolation was between –25 to –30 dB's showing that the device was non-reciprocal, unlike the conventional TWF.

4.5.2) Output power

One of the main interests in the development of travelling wave structures was for medium RF output power amplification over a wide bandwidth which could be used as a solid-state driver amplifier for travelling wave tube (TWT) amplifier technology.

To understand the power-handling capability of a travelling wave device it was necessary to investigate the concepts which are used in the evaluation of conventional class A RF power transistors **[I16].**

$$P_{rf} = I_f [V_B - V_k - V_p]/8 \qquad (4.5.2.1)$$

Where P_{rf} is the RF output power in watts, V_B is the gate-drain breakdown, V_k is the knee voltage and V_p the pinch-off voltage (normally $V_B >> V_k$ and V_p), and I_f is the maximum current under forward gate bias.

The product $[V_B - V_k - V_p]$ will depend on the semiconductor material, the number of defects, gate drain separation and is equal to the maximum allowable voltage swing on the output of the transistor. The current I_f in a conventional power FET is increased by increasing the total gate-width (W) of the transistor. In a practical device a large total gate-width (W) is obtained by paralleling up many unit gates (w_{unit}). The unit gate-width (w_{unit}) is designed to be smaller than the operational wavelength, and a design guide is given by the distributed model $\lambda_g/20$ (see section 3.6.2). To a first approximation, the transistor input impedance consists of a capacitor in series with a resistor. As the transistor total width W is increased the capacitance increases and the resistor decreases. Ultimately the circuit will become more difficult to match over a bandwidth, thereby limiting the total width of the transistor. The overall geometrical size of the transistor chip will also limit geometrical size of the device, as the input signal will excite different phases at each point feeding the unit gate-width.

In a travelling wave transistor (TWF) the voltage grows on both the drain and gate electrodes when the 'growing wave' propagates. The gate-drain breakdown (VB_{gd}) will occur at the output section of the travelling wave device and will depend on the algebraic

sum of the gate and drain output voltages. In both the TWA and LGT the gate and drain are in anti-phase at the output so that the voltage on either electrode will be less than breakdown when it occurs. This effect is worse in the TWF where the magnitudes on the gate and drain voltages are almost equal.

$$P_{rf}(TWFET) = 2\{v^2/2R_{out}\} \text{ where } v = v_d = v_g \approx V_{Bgd}/2 \qquad (4.5.2.2)$$

$$P_{rf}(LGT) = v^2/2R_{out} \text{ where } v = v_d \approx V_{Bgd}/2 \text{ as } v_g = 0. \qquad (4.5.2.3)$$

It can be seen that both will give a similar output power performance provided the characteristic impedances have been designed to be similar. However, for the examples of the TWF and LGT experimentally investigated, the TWF had lower characteristic impedance. The lower impedance would suggest that it would give a slightly higher output power performance than the LGT. A more complete analysis of the TWF output-power capability was published by Rozzi in 1995 [80].

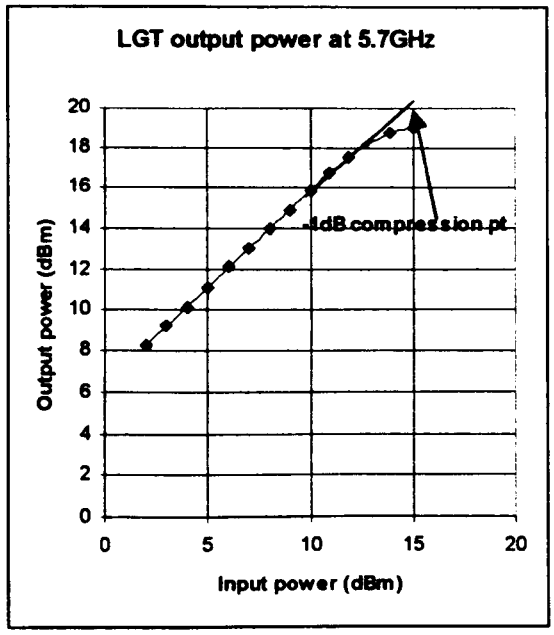


Figure 47 Output power for a five section LGT

The above simple model indicates that both the TWF and LGT will give a very much lower output power when compared with a conventional power FET with the same total gate-width as its output impedance will be much lower.

This can be seen in Figure 47, which shows an experimental plot of output power verses input power for a 2.0mm LGT device, giving a maximum measured output power of less than 100mW **[I17].** Whereas, a conventional GaAs power MESFET with 2.4mm of total gate periphery will give an RF output power of the order of 2 Watts, but only over a relatively narrow bandwidth **[B8].**

The 2mm LGT consisted of 5 active sections **[B13, I17]** see Figure 48, and each active section was approximately 100 microns.

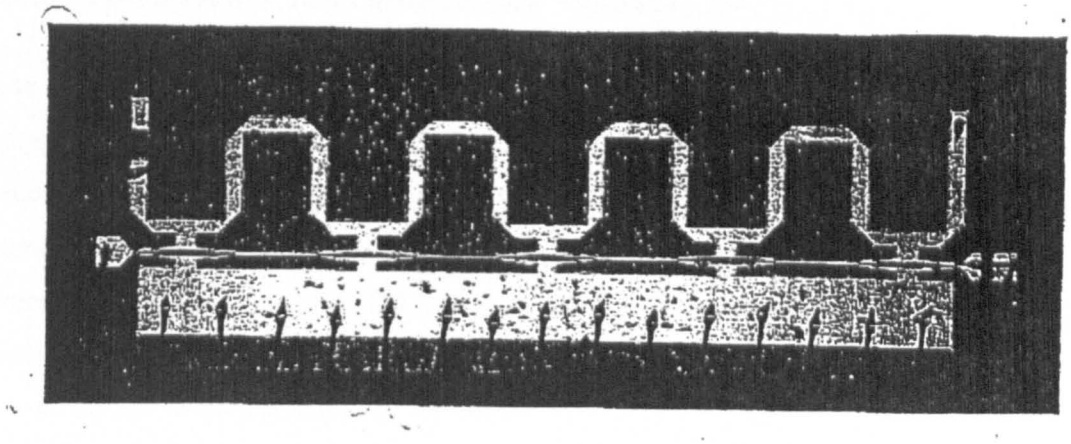


Figure 48 Five section LGT

If the standard 1W/mm for GaAs [84] FET is used, then for 100 microns of gate-width approximately 0.1 Watt output power should be realised, which is close to the experimental value of 19dBm at the –1dB compression point obtained for the LGT.

Theoretically travelling wave structures will deliver the output power over a very wide-bandwidth, the cut-off frequency being determined by the periodic distributed nature of the capacitive and inductive elements i.e $f_t = 1/(\Delta L \Delta C)^{0.5}$.

Therefore, for a travelling wave structure designed to operate directly into a 50-Ohm load the output power capability will be a function of the drain gate breakdown voltage (VB_{DG}). Wemple [41] has shown that this is a direct function of the avalanche breakdown field (E_a) of the semiconductor. Recent advances in the material growth technology of

wide-band gap semiconductors, for example Gallium Nitride GaN with a breakdown avalanche field approximately 10 times higher than for GaAs will theoretically give the potential of an RF output power 100 times higher than for GaAs **[C4]**, provided the extra heat generated can be efficiently dissipated. This would give the potential of medium output-powers (0.1 to >1 Watt) and octave bandwidths. The characteristic impedance of the structures could also be tailored to the application/system giving the potential of lowering the impedance and increasing the output power further

4.5.3) Third Order Intermodulation Product

The third-order inter-modulation product of the 2.0mm LGT was measured at the –1dB compression point using a single tone signal at the input, which was separated from a second input signal by approximately 1 MH_z **[I17]**. The amplitude of both the input signals was equalised. The total two tone input power was then reset for the –1dB compression point and the C/I ratio of the third order inter-modulation products monitored on the spectrum analyzer. The measured third order product was between –20 to –26 dB below the fundamental frequency.

4.5.4) Noise performance

The minimum noise figure of the 2.0mm LGT was measured over the bandwidth (2 to 8 GH_z), using a semi-automatic gain/noise figure analyser [ETN 2075], and at two different channel currents $I_{dss}/2$ and $I_{dss}/4$, and the results are shown in Figures 49 and 50 respectively.

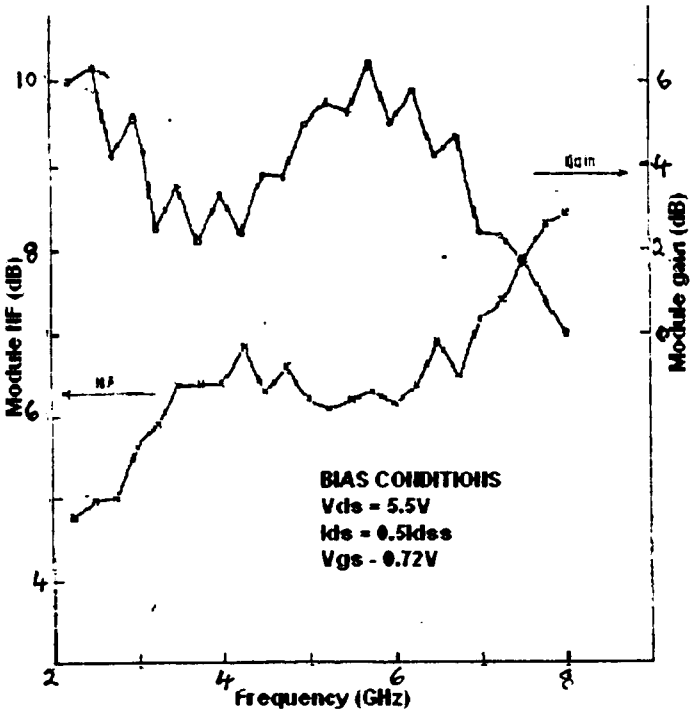


Figure 49 Minimum noise figure ($I_{dss}/2$)

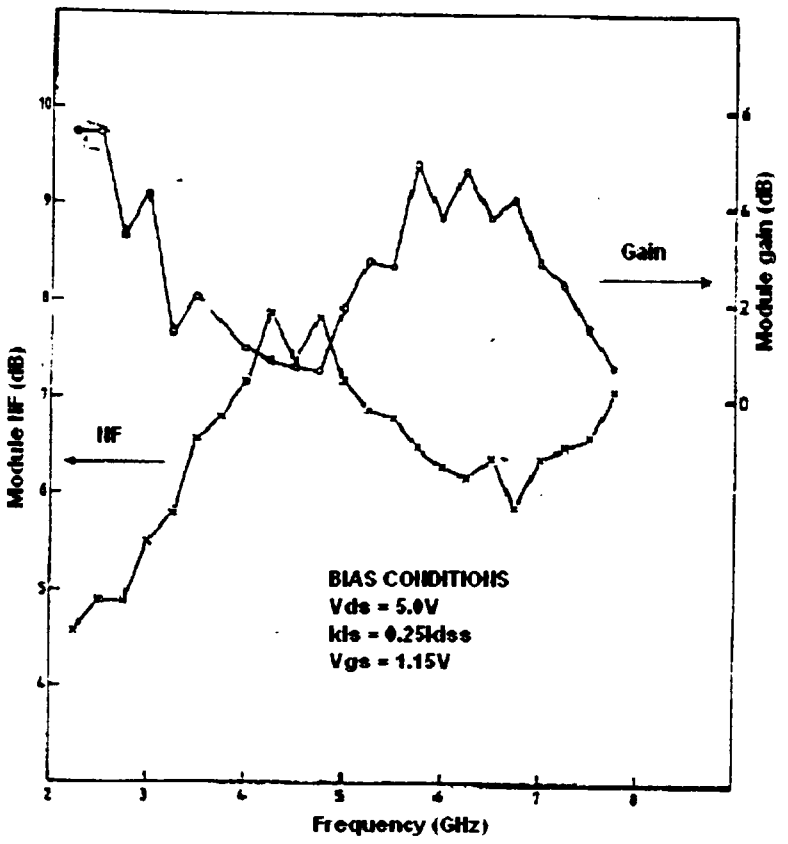


Figure 50 Minimum noise figure ($I_{dss}/4$)

The minimum noise figure appears to be very similar for both I_{ds}/I_{dss} = 50% and 25% respectively. The comparison was made at the frequency of maximum gain, as it represented the point of lowest mis-match [I17].

With increasing gate bias and therefore reducing I_{ds} both noise figure and gain deteriorated which is contrary to that usually observed for conventional MESFETs. The gain plots in particular, show a fine ripple with a period of approximately 1 GH_z, which is thought to be due to mis-matching of the drain and gate idle electrodes resulting in reflections along the gate and drain transmission lines.

The noise performance of the distributed TWA has been shown to be improved significantly by using low noise HEMT devices [83]. To the authors' best knowledge a noise model for the travelling wave FET which supports a growing wave has not been analyzed.

4.6) Conclusions

The linear gate transistor capability has not been fully explored due to short-comings in the available technology in 1985 when the device was conceived. In particular, the development of device technology has significantly improved over the last three decades, with the realization of short gate-lengths (typically 0.15 microns) with very low RF resistance [49]. Also, the rapid development of the HEMT would give an enhanced transconductance, greatly improving the gain bandwidth capability. Recent publications have shown that extremely wide bandwidth products are now feasible, for example J. Pusl et al [75] reported a monolithic capacitive coupled TWA with 340GH_z gain-bandwidth product, using 0.15 a micron gate-length InGaAs/InAlAs HEMTs. The recent advances in wide band-gap HEMT devices would enable very respectable output powers to be obtained, and is being explored as a TWA in the USA [85].

4.7) Recommendations

1) Develop low resistance (<2 Ohm/mm) short gate length (.25 microns) structures

2) Extend the computer model to include non-linear effects and noise modelling.

3) Optimise the structure for fabrication on wide-band gap material to enhance the output power capability but maintain an impedance of 50 Ohms over a multi-octave bandwidth.

INDUSTRIAL REPORTS supporting the work I9,I,10,I11,I12,I14,I15,I16,II17,I18,

5) WIDE-BAND GAP SEMICONDUCTORS

5.1 Introduction

Wide band-gap semiconductors have been considered for high power applications over a number of years, as the ideal output power of a FET structure is proportional to the square of the avalanche breakdown field E_a [49] and can be expressed (5.1.1):

$$P_{rfmax} = \varepsilon_0 \varepsilon_r L_g E_a^2 W v_s / 16 \qquad (5.1.1)$$

ε_0 = free space permittivity

ε_r = relative permittivity

W = total gate width

L_g = gate length

E_a = avalanche breakdown field

v_s = saturation velocity

The equation (5.1.1) shows that the maximum output power from transistors with identical geometry is dependent on the semiconductor used. Table 5 summarises the properties of some of the common semiconductors used in the fabrication of microwave frequency FET devices, including two recently introduced wide-band gap materials Gallium Nitride (GaN) and Silicon Carbide (SiC).

TABLE 5

Semiconductor	E_a (V/cm)	v_s (cm/sec)	ε_r
Silicon	$2x10^5$	$0.9x10^7$	11
Gallium Arsenide	$4x10^5$	$1.0x10^7$	12.4
Indium Phosphide	$5x10^5$	$0.9x10^7$	12.5
Silicon Carbide	$4x10^6$	$1x10^7$	10
Gallium Nitride	$5x10^6$	$2.5x10^7$	8.9

From table 3 it is seen that GaN transistors will give considerably more RF output power than devices fabricated on GaAs, InP, or Si, which is primarily due to its very much higher avalanche breakdown field (E_a). To-date output powers in excess of 32W/mm [15] have been reported from small area AlGaN/GaN HEMT devices compared with the best laboratory result of around 1.5W/mm for a GaAs device.

The maximum output power density in class A operation can be estimated for the GaN HEMT by considering the following:
$P_{RF}/mm = qN_c v_{sat} a[V_{Bgd} - |V_P| - V_K]/8 \approx 50W/mm$, where it was assumed $v_{sat} = 1.5x10^5 m/sec$ (present work suggest that the maximum experimental saturation velocity is of the order $1.32x10^5 m/sec$ [86]), $V_{GDB} = 60$ Volts, and the sheet carrier concentration is approximately $7x10^{12}$ atoms cm^2. The reported maximum sheet density is 10^{13} atoms cm^2 [87].

The predicted maximum output power density of 50W/mm is similar to a figure published by Eastman [88] at Cornell University. It is unlikely, experimentally, to obtain such a high RF power density, as the minimum DC power dissipation density will be in excess of $100W/mm^2$, assuming an ideal class A power added device efficiency of 50%.

The rapid interest in GaN transistors has occurred within the last decade, as material of sufficiently good quality for the fabrication of microwave transistors became available from early 1990. Interestingly, the first GaN crystals were synthesised in 1946 [89]. Presently the GaN active layers are grown on sapphire or silicon carbide SiC, as there is no naturally occurring crystal of GaN. Silicon Carbide gives the closest lattice match to GaN and has very good thermal properties and therefore makes an ideal substrate for power transistor's **[C4].** Recent work by Nitronex (USA) has shown the feasibility of fabricating GaN layers on silicon; this technology is now being pursued by QinetiQ (UK) as it may lead to cost effective high-performance power-transistors for both commercial and military applications.

The material offers many advantages for the design of high power RF/microwave transistors and therefore most of the international research/development has been aimed towards the medium/high power market. It was therefore surprising, when very low minimum noise figures were also obtained from GaN HEMT devices [90]. This result suggested the feasibility of both very high power and low noise GaN based FET devices. Further, the high breakdown fields associated with GaN HEMT devices may eventually lead to small-signal low noise devices with high drain gate breakdown characteristics, giving the possibility of high cw and pulse burn-out properties. The devices therefore represent an interesting contender to GaAs and InP based transistors in some low noise front-end applications where limiter diodes would normally be used.

The research work carried out by the author was aimed at developing small and large signal GaN transistor models, as well as the development of simple minimum noise analysis, based on the Fukui model.

5.2) DEVELOPMENT of a SMALL SIGNAL EQUIVALENT CIRCUIT MODEL

To further the understanding of the AlGaN/GaN HEMT, a small signal equivalent circuit model was developed and the variation of the elements with bias were investigated over a wide range of transistor bias conditions.

To undertake the investigation an AlGaN/GaN HEMT, which was fabricated at the QinetiQ facility in the UK, was used. The transistor consisted of a nominal 0.25-micron gate-length with a metallised T-profile in order to minimise the parasitic gate resistance (R_g). The total gate-width was 100 microns and consisted of two unit gate-widths of 50 microns in a 'pi' configuration (similar to the original C1 structure). The structure was fabricated on a SiC substrate with AlN buffer region and passivated with silicon nitride (Si_3N_4) **[C1 & C3].**

The s-parameters of the transistor were measured by QinetiQ from 0.1 to 50GHz, using an Agilent network analyzer connected to an RF probe-station. Each set of s-parameters was measured at a separate bias point, using a range of drain source voltage (V_{DS}) from 0

to 40 volts, and for a range of gate source voltages (V_{GS}) from –8 to 0 volts. The pinch – off voltage (V_P) was approximately –6.5volts.

A de-embedding procedure was developed following [42, 55, 91] and the methodology is summarized below:

a) Measure s-parameters from 0.1 to 50GHz. Bias condition (V_{DS} = 0V and V_{GS} = -8V)

b) Transform to y-parameters and determine the gate (C_{gpad}) and drain (C_{dpad}) parasitic geometrical capacitance. The parasitic capacitance associated with the depletion layer through the AlGaN and 2D-electron gas layer is also determined.

c) The three leakage resistances can also be determined associated with the gate source capacitance (C_{gs}), gate drain capacitance (C_{gd}) and drain source capacitance (C_{ds}).

d) Transform to z-parameters. Bias condition (V_{DS} = 0V, V_{GS} =0V).

e) Four equations representing the real part of the z-parameter can be found. These can be extrapolated back to DC and solved simultaneously to obtain an estimate for the source resistance (R_S = 8.5Ω), drain resistance (R_D = 10Ω), and gate resistance (R_G = 0.46Ω). Note the source resistance is only an estimate.

f) A best-fit on Z_{11} was then performed to 10GHz to obtain a value of 0.03pH for the gate inductance (L_g), which is dependent on the depletion layer under the gate and for a HEMT device can be considered a constant, according to Ladbrooke [91]. Both the source and drain parasitic inductance were considered to be very small and therefore neglected at frequencies to 10GHz.

g) Transform to y-parameters and extract the elements of the intrinsic equivalent circuit model for each bias condition, using the following expressions:

1) $C_{gd} = -Im(Y_{12f})/\omega$

2) $C_{ds} = [Im(Y_{22f})/\omega] - C_{gd}$

3) $C_{gs} = [Im(Y_{11f})/\omega] - C_{gd}$

4) $g_{ds} = Re(Y_{22f})$

5) $gm = [(gmr)^2 + (gmi)^2]^{0.5}$ where $gmr = Re(Y_{21f}) - Im(Y_{21f}).R_{ch}.C_{gs}.\omega - C_{gs}.C_{gd}.R_{ch}.\omega^2$

$$gmi = Re(Y_{21f}).R_{ch}.C_{gs}.\omega + Im(Y_{21f}) + \omega.C_{gd}$$

6) $R_{ch} = \{1 - [4(Re(Y_{11f})^2]/\omega^2.C_{gsf}^2\}/2Re(Y_{11f})$

A novel approach for extracting a more exact value for the source resistance and over a range of bias conditions was developed **[C2]**. The extracted values indicated that at a high V_{gs} the access resistance appears to be lower, which would suggest that the carrier conduction is spread over a larger cross-section of conducting channel. The increase in cross-section may be due to a parallel conduction path to the 2-D electron gas layer and the carriers in both regions having similar velocities. The parallel conduction may be in either, the GaN or the AlGaN layer [92, 93].

The variation of C_{gs}, C_{gd}, C_{ds}, R_{ds} and gm with bias conditions, and a number of interesting features can be identified. For example, the measurements show that the intrinsic transconductance peaks very close to pinch-off, Figure 51, corresponding to the bias setting where maximum ft was observed **[C1]**, and the variation with V_{ds} is relatively small except at very high V_{gs}, for example 0 Volt. For the conventional HEMT the

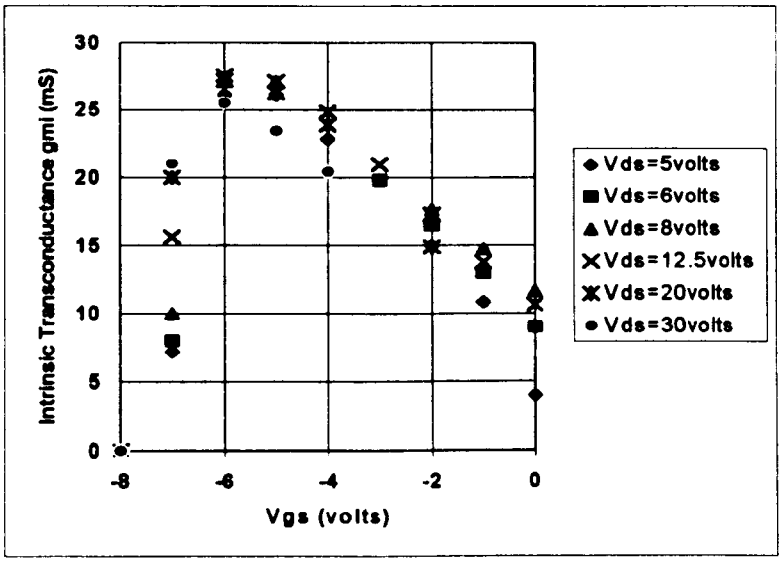


Figure 51, variation of intrinsic transconductance with V_{ds} and V_{gs}.

reduction in the transconductance is explained by considering the existence of a parasitic MESFET in the wide-band gap layer; for this device the AlGaN layer. This is normally accompanied with a reduction in the input C_{gs} gate source capacitance [91] at high V_{gs}, which was not observed to any great extent in the AlGaN/GaN HEMT, Figure 52. The increase in C_{gs} with high V_{ds} is thought to be due to the extension of the depletion layer under the gate with increasing drain gate field **[C1]**.

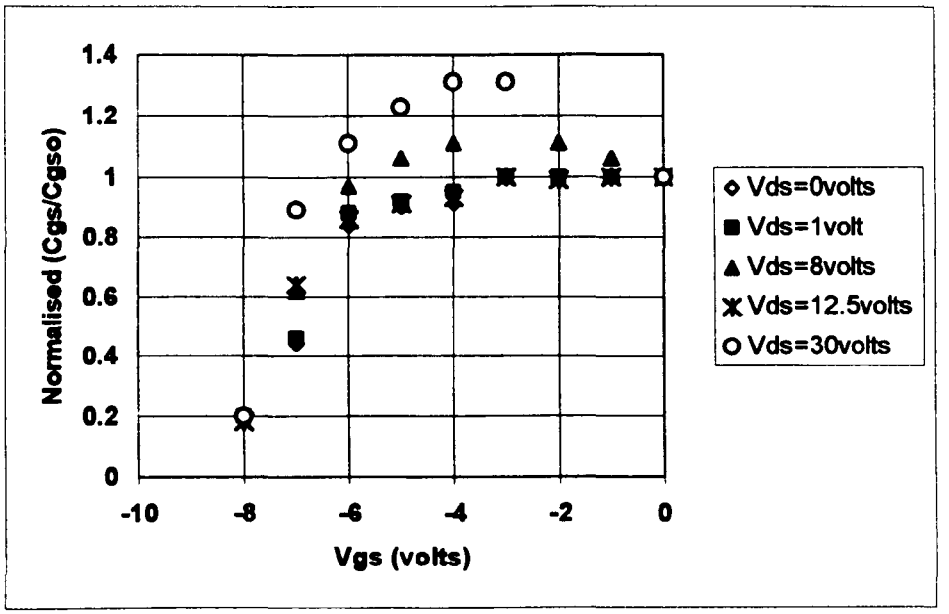


Figure 52, (C_{gs} variation with V_{ds}, V_{gs})

The pseudo quasi-static model for the HEMT is also being investigated, as the charge at each electrode can be considered separately. For example, the drain gate capacitance (C_{dg}) will take into account the variation in charge in the drain as the gate voltage is changed, which will be different from the gate drain capacitance (C_{gd}), due to variation in the gate charge as the drain voltage is changed [42]. The expressions to extract the

intrinsic transistor parameters from the de-embedded y-parameters obtained from the measured s-parameters are given below [42]:

$y_{11} - y_{12} = (R_{ch} + 1/j\omega C_{gs})^{-1}$

$-y_{12} = (R_{gd} + 1/j\omega C_{gd})^{-1}$

$y_{22} - y_{12} = g_d + j\omega C_{sd}$

$y_{21} - y_{12} = g_m - j\omega C_{dg} + j\omega C_{gd}$

$g_m = [(Ry_{21} + Ry_{12})^2 + (Iy_{21} + Iy_{12})^2]^{0.5}$

Experimental work by the author is in progress looking at the differences between the extracted intrinsic parameters of a GaN HEMT for 'pseudo' and non quasi-static models. The parameters as a function of bias conditions are being used to set-up a large signal model, based on the Angelov model.

5.3) NOISE PERFORMANCE of GaN HEMT.

A full review of GaN microwave HEMT was published **[C4].** In the article the author made the first published prediction of the NF_{min} of the GaN HEMT transistor, using the Fukui analysis, presented in section (3.5.3).

$$NF_{min} = 10\log_{10}\{1+4\pi F v_s^{-1}[\{L_g I_{opt}((R_{S1}+R_C)+R_g)\}/E_c]^{0.5}\}\,dB \qquad (5.3.1)$$

To predict NF_{min} as a function of frequency, realistic values for the different parameters of the transistor were required. In particular it can be seen that the NF_{min} is inversely proportional to the saturation velocity, v_s.

The very limited experimental results [62, 63] available for NF_{min}, indicate that the optimum current (I_{opt}) is 20% to 25% of I_{dss}, which is similar to earlier findings on GaAs transistors. Subsequent work by another research group on GaN transistors has shown that for NF_{min} I_{opt}/I_{dss} = 15% [94].

Both published and experimental data was used to determine a value for the critical field E_c and saturation velocity v_s **[C3].** The initial work **[C3]** indicated a $v_s = 1.19\text{x}10^7$cm/sec

which would correspond to an intrinsic cut-off frequency (f_{ti}) of 76GH_z for a 0.25 micron gate-length GaN transistor. This figure was calculated using the ratio between the saturation and peak velocity, from Monte Carlo simulation and was found to be approximately 0.62, table 1, page 2, **[C3]**. The ratio was then used to find the value of the saturation velocity, knowing the experimental peak velocity from Wraback [95].

The saturation velocity is dependent on a number of factors which include device parasitics, temperature effects due to self-heating, parallel path conduction and scattering mechanisms within the material. The more accurate extraction of the intrinsic saturation velocity (v_{si}) from the intrinsic device has been explored by the author in **[C1]**. This was undertaken by measuring the s-parameters to 50GHz of a 0.29 micron gate-length AlGaNGaN HEMT with a maximum extrinsic f_t = 37GHz. The intrinsic saturation velocity was extracted from the de-embedded s-parameters over a wide range of bias conditions, and therefore only dependent on scattering mechanisms within the material, temperature due to self-heating and any parallel conduction path through the device. The derived expression by the author for the extraction of the intrinsic saturation velocity is given by:

$$v_{si} \approx \frac{(L_g + \sigma) g_{mi} C_{gsi}(V_{gs}, V_{ds})}{C_{gsi}(V_{gs}, 0)\sqrt{C_{ggi}(V_{gs}, V_{ds})^2 - C_{dgi}(V_{gs}, V_{ds})^2}} \qquad (5.3.2)$$

The equation (5.3.2) accounts for the gate-edge fringing-effect, elongation of the depletion layer under the gate at high drain gate electric field, and asymmetry of the gate and drain charge, by the difference in the gate drain capacitance C_{gd}, and drain gate capacitance C_{dg}. The maximum extracted intrinsic saturation velocity was 1.1×10^5m/sec, which is lower than Monte Carlo simulation, indicating other mechanisms are present, for example parallel path conduction and scattering mechanisms, if self-heating effect is neglected.

Other published experimental work [96] has shown a f_t of 120GH_z for a 0.15 micron gate-length HEMT, giving a maximum saturation velocity of the order 1×10^5m/sec. The present, lower than expected f_t values may be a result of high strain in the material causing high levels of defects during material growth [97], or subsequent device processing [98], and high drain gate electric field causing a fringing region to extend well

beyond the gate metallization [99], which has now been explored and included by the author **[C1]**.

The gate resistance R_g required in the minimum noise expression (5.3.1) was calculated for a 0.25 micron gate length 'pi' structure with a total gate width of 100 microns using the expression (3.3.1.1).

The total source resistance R_s was assumed to consist of two parts, the contact resistance R_c and the resistance of the semiconductor R_s'. For simplicity, if the assumption is made that R_c is similar to that obtained for GaAs, then R_s will differ by approximately the ratio of the mobilities between GaAs and GaN. This would suggest that the parasitic source resistance R_s will be 4 to 6 times greater in the GaN transistor when compared with the GaAs device.

In comparison with experimental NF_{min} of 2dB at 20 GH_z **[C3]** for a GaAs MESFET and knowing the measured R_{stotal} was approximately 3 to 4 Ohm. A comparable GaN transistor will have R_s between 12 to 24 Ohm and NF_{min} of 1.1 dB at 20 GH_z. This is an interesting result as it suggests that the intrinsic noise performance of a GaN HEMT is lower than that for a GaAs HEMT **[C3]**. Some recently published experimental work by the University of Illinois [100] has shown NF_{min} = 0.42dB at 8GHz from a GaAlN/GaN HEMT at room temperature.

Note the breakdown voltage of these devices is much higher than for GaAs transistors, giving the potential, in some applications, of low noise front-ends without limiter stages.

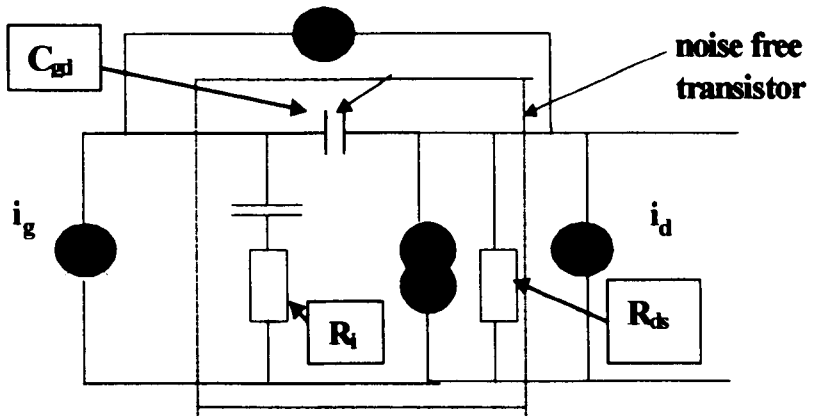
5.4 A More Complete Analytical Noise Model for GaN HEMT Devices.

Gallium Nitride is normally grown on a substrate of different material introducing a lattice mismatch and there can also be significant differences in the thermal expansion coefficient (TEC) which will cause bowing of the substrate. These will introduce bulk defects into the semiconductor as well as surface defects in between the gate and drain electrodes of the transistor. The defects will have a significant effect upon the microwave

performance of the transistor, giving rise to dispersion [101] in the IV characteristics which is already a significant area of research in GaN power transistors. The material defects will influence other transistor parameters, for example the cut-off frequency (f_t) **[C1]**, and the output conductance (g_{ds}).

The above parameters will have an effect on the transistor intrinsic noise sources (Figure 53) and subsequently the minimum noise figure as a function of frequency; a very simple analytical approach to investigate the above has been developed **[C2]**, by the author.

Figure 53 intrinsic noise model



To simplify the discussion, only the intrinsic noise performance was investigated, therefore the extrinsic source resistance R_s, gate resistance R_g and drain resistance R_d were neglected.

The minimum noise figure is given by:

$$NF_{min} = 1 + 2(f/f_t)[PR(1-C^2)]^{0.5} \qquad (5.4.1)$$

P = drain noise coefficient

R = gate noise coefficient

C = noise correlation coefficient

The above expression does not take into account the capacitive coupling between the drain and gate (C_{gd}), or gate leakage (I_{gc}) due to semiconductor surface defects and the high electric fields between the gate, and drain electrodes.

The drain noise $\langle i_d^2 \rangle$ is is normally the most significant, of the noise sources and dependent on the channel diffusion current. It has already been discussed in section

(3.5.3) that the gate noise $\langle i_g^2 \rangle$ influences the drain noise $\langle i_d^2 \rangle$ even at very low frequencies as the two noise sources are correlated. Therefore, under optimum bias conditions, a reduction in $\langle i_d^2 \rangle$ is expected which is determined by the magnitude of the correlation factor C. As the parameters P, R and C are biased dependent; the NF_{min} remains linearly dependent on frequency. The physical mechanism for the generation of the gate noise is uniform due to the direct correlation with the noise sources within the channel. However, if gate noise is generated, for example by leakage effects at the surface of the semiconductor, this extra noise within the device will not be correlated, and therefore will not influence C the correlation factor or the induced gate noise.

It has already been shown by Delagebeaudeuf [61] that it is a reasonable approximation to take the diffusion coefficient D, parallel to the electric field under the gate, as the constant low field value $D \approx kT_0\mu/q$, and assume the perpendicular diffusion coefficient D is zero. Where μ is the low field carrier mobility and q the electronic charge; by considering that the transistor is biased to the knee point V_K and the critical field E_c is at the edge of the gate nearest the drain, the mobility under the gate is a constant and the expression already presented in section (3.5.3) can be used:

$$P = I_{ds}/(g_{mi}E_cL_{eff}). \qquad (5.4.2)$$

P has been shown to give reasonable agreement with measured values for GaAs based transistors see section (3.5.3).

This may be expressed as the drain noise spectral density $S_{id}(f) = 4kTg_{mi}P\ A^2/Hz$,

The band structure for GaN is more complex than GaAs, giving a velocity-field (V-E) characteristic which to a first order can be represented by a simple piece-wise model see (page 3, Figure 2 **[C2]**). It is well known that strain will reduce the band-gap [102] and high levels of defects will substantially modify the internal electric field [102] within the semiconductor. Couple this with large gate fringing effects **[C1]** the actual 'device' V-E characteristic could be substantially modified. In the low field region the mobility of un-doped GaN at room temperature is of the order of 1100V- sec cm^2 [103], giving rise to a saturation velocity of around $1x10^5$ m/sec, which is similar to the experimental extracted value **[C1]**. The typical knee voltage (V_K) for a GaN HEMT is 4 to 5 volts and with a nominal source drain spacing of 3.0 microns the electric field parallel with the gate will be of the order of 20kV/cm. Recent published work [104] has shown that the drift

velocity saturates at low fields 20kV/cm and is thought to be partially due to self-heating effects within the transistor.

Using the above results and for a 0.41 micron gate-length HEMT, $S_{id}(f) = 6.64x10^{-22}$ A^2/H_z which agrees well with an experimentally measured value of $4.0x10^{-22}$ A^2/H_z published by the University of Cornell [105]. It is interesting to note that for a similar geometry device fabricated on GaAs, the calculated noise spectral density $S_{id}(f) = 2.3x10^{-21}A^2/H_z$ is a factor of 6 higher.

With increasing frequency the experimental NF_{min} of GaAs transistors is seen to depart from the linear frequency response, which is partly or wholly attributed to the gate-drain feedback capacitance, see section (3.5.3 and 3.6.2).

$$\langle i^2_{d0} \rangle = \langle i^2_d \rangle.[1 + (f/f_B)^2] \qquad (5.4.3)$$

Where $f_B = g_{ds}/2\pi C_{gd}(w)$ and g_{ds} is the output conductance of the transistor

Combining equations (5.4.2) and (5.4.3) a more complete expression for P can be obtained

$$P = [I_{ds}/g_{mi}E_cL_{eff}][1 + (f/f_B)^2] \qquad (5.4.4)$$

Provided $f < f_B$ then P is frequency independent, and above f_B, P becomes frequency dependent and will be a function of both device geometry and the quality of the buffer layer and interface.

To a first approximation, f_B is increased by reducing the gate-length, gate width (**[C2]** and section 3.6.2) and assuming the carriers have reached saturation in the buffer region. In reality f_B can be determined by de-embedding the intrinsic values of C_{gd} and g_{ds} from the measured s-parameters.

Gate leakage has been included in the noise analysis of the GaN HEMT **[C5, C4]**, based on the published paper by Shin [106] who included gate leakage current I_{gl} as an additional shot noise source $\langle i_{gs}^2 \rangle = 2qI_{gl}\Delta f$ between the gate and drain contacts. This noise originates from the reverse leakage current of the Schottky barrier at the high electric field region near the drain contact, high surface defect densities, and poor metal to semiconductor interface. The spectral density of the shot noise source is $S_{igl}(f) =$

$2qI_{gl}\Delta f$ and is typically $< 10^{-23}$ A^2/H_z; provided $S_{igl}(f) << S_{id}(f)$ and the higher order terms are neglected, Shin [106] derived the following expression for NF_{min}:

$$NF_{min} = 1 + 2f/f_t\sqrt{(PR_i)}[1 + (f_c/f)^2]^{0.5} \quad (5.4.5)$$

By assuming $R_i \approx 1/(2g_{mi})$, then to a first approximation $f_c = f_t\{2qI_{gl}/[g_{mi}2kT]\}^{0.5}$

Combining equations (5.4.4) and (5.4.5) gives the minimum noise figure NF_{min} as:

$$NF_{min} \approx 1 + 2(f/f_t)\{[I_{ds}/2g_{mi}E_cL_{eff}][1 + (f/f_B)^2][1 + (f_c/f)^2]R[1-C^2)]\}^{0.5} \quad (5.4.6)$$

To investigate the effects of f_B and f_c on the performance of the GaN HEMT the variation of I_{gl}, g_{ds}, and C_{gd} with bias voltage (V_{ds} and V_{gs}) were experimentally determined **[C2]**. Figures 54 and 55 show the variation of gate-leakage and output drain source resistance ($R_{ds} = 1/g_{ds}$) as a function of gate and drain bias.

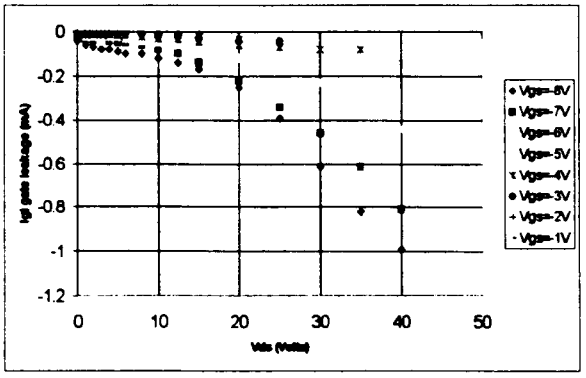


Figure 54, gate leakage as a function of bias conditions.

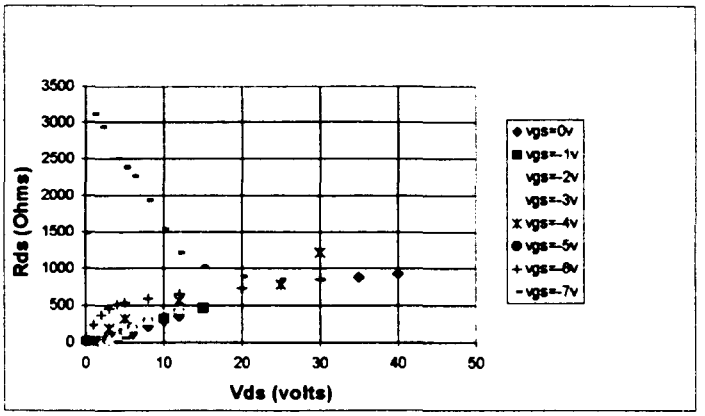


Figure 55 R_{ds} as a function of bias conditions

Figure 55 shows that when the device is pinched-off, R_{ds} reduces with increasing V_{ds}, indicating that carriers are being generated within the buffer interface layer. As V_{gs} is increased R_{ds} increases with V_{ds}, unlike the InP metamorphic HEMT where R_{ds} still decreases. The decrease in R_{ds} in the metamorphic HEMT was explained by the onset of impact ionization, leading to a further source of noise in the channel. Therefore, it appears safe to assume that in the GaN HEMT this noise source can be neglected.

The intrinsic gate drain feedback capacitance was measured for different V_{ds} and V_{gs} and using the expression for $f_0 = g_{ds}/2\pi C_{gd}$ was plotted as a function of (V_{ds} V_{gs}) and is given in (figure 6 **[C3]**).

Using the above model it was possible to explain the different published NF_{min} results [90, 94, 100] versus frequency from a number of organisations **[C3]**. The NF_{min}/frequency profiles, included flat [3, 7] and linear responses [4]. While one publication contained a departure, in which the experimental NF_{min} when linearly extrapolated to 0dB, intersected the frequency axes at approximately 6 GHz [3]. This was a surprising result as it suggests the feasibility of a very low noise figure in C-band. All the published noise results indicate that the transistors have a very high breakdown voltage compared with GaAs.

CHAPTER 6: CONCLUSIONS

The work presented gives an overview of the authors' involvement in the research and development of solid state devices suitable for the amplification of microwave signals in the last 35 years.

The research work started with the design of TRAPATT diodes suitable for use in reflection type of amplifiers, leading to a three-stage, 10 Watt pulsed, class C power-amplifier working in X-band. The work highlighted the difficulties in the design and realization of practical amplifiers in the X and J frequency bands, and firmly placed the TRAPATT diode for applications limited in the lower L and S frequency bands.

By the end of the seventies and the beginning of the eighties the major thrust in the active microwave device arena was the gallium arsenide MESFET, and the work by the author played a part in the understanding and development of this transistor.

The authors' research work led to the realization of a GaAs MESFET structure (C1) with low parasitic elements enabling state of the art measured noise performance in Q-band, the results were published in the IEDM 1981 **[B15].** Variants of the C1 device structure have been used by a number of organizations, including Marconi where it was used as the transistor test vehicle for HEMT devices fabricated on wide-band gap material.

Microwave characterization techniques were also developed to enable more accurate measurement of s-parameters and the de-embedding of the circuit elements to realize the small signal equivalent circuit model of the transistor. Techniques for measuring and improving the measurement of high frequency minimum noise figures were also developed. Minimum noise figures were measured to frequencies in excess of 33GHz and high frequency test circuits and interfaces were developed. The measurements high-lighted the departure of the minimum noise figure from the Fukui noise theory, with increasing frequency. The frequency at which the departure took place was found to be dependent on the unit gate-width of the transistor and were probably some of the first measurements of the type to be reported.

The concept of distributed effects due to mutual coupling between the electrodes was investigated by the author and good agreement was found with the experimentally measured s-parameters and lumped equivalent circuit model to approximately 20GHz.

Above this frequency, the distributed model was directly compared with the extrapolated s-parameters derived using the lumped equivalent circuit model and the main departure was in the magnitude of s22, and the phase of s21. Otherwise the magnitude and phase of the other s-parameters remained very similar. The results indicated that the lumped circuit model for a 'standard' type of FET structure would be reasonably well represented by the lumped equivalent circuit model. This certainly has been verified by a number of workers, as the lumped circuit model is used to very high frequencies >100GHz, and good agreement with experiment is obtained, provided the de-embedding exercise is carried out with great care.

The work on distributed effects led to experimental realization of the travelling wave field-effect transistor (TWF), the phase of the waves along the gate and drain electrodes were equalized by using drain/source over-layer capacitors. The transistor was fed by a miniature balun circuit and the device was found to support a growing wave, and the reciprocal nature of the device gave rise to Fabrey Perot type of oscillation. The author believes that this was the first reported **[B12, I10]** experimental evidence of a growing wave, in a GaAs transistor. The reported work showed that the TWF transistor was impractical for any real application and (Oxley, Holden) proposed a new traveling wave transistor structure known as the Linear Gate Transistor (LGT) which was non-reciprocal and support a growing-wave. The device balanced the phase along the gate and drain lines by meandering the drain line similar to the travelling wave amplifier (TWA) this increased the characteristic impedance of the drain electrode giving rise to an increase in the active gain per periodic section of the distributed device when compared with the TWF. In the active region of the device, the gate and drain lines were brought into close proximity enabling coupling between gate and drain electrodes, thus feeding energy back into the gate line and in phase with the original input signal thus providing conditions for the growing wave. Experimental devices were fabricated and the gain was measured over a wide bandwidth (1 to 12GHz). Theoretical analysis indicated that to obtain the growing-wave, a narrow and very low resistance gate structure was required. At the time of the research the technology was not sufficiently mature to enable the fabrication of long, narrow (<0.5 micron) low resistance gate structures.

PAGE MISSING IN ORIGINAL

CHAPTER 7: FUTURE WORK

The presented work gives a number of opportunities for future research, which are highlighted in this chapter.

Two terminal devices:

To-day, the two-terminal device is still found in some specialized applications, for example the TRAPATT diode in proximity fusing and the Gunn diode in the 77GHz automobile active radar **[C8].** It is perhaps true to say that the two-terminal device has been pushed into niche areas, for example millimetric (40 – 1.9THz) wave and pulsed high output-power applications. In very recent years both these niche areas are being challenged by the microwave high electron mobility transistor. Future work, could include a feasibility investigation in obtaining high output-power into the high milli-metric frequency band from two terminal transfer electron devices fabricated using wide-band gap materials, for example GaN.

Three terminal devices:

The frequency at which the minimum noise figure departs from the Fukui noise theory has been shown experimentally to be dependent on the unit gate-width. The author explained the departure as a result of distributed effects within the transistor. Other authors, for example Cappy, have explained the observed effect as a result of the channel noise having a frequency dependence due to the gate drain capacitance, C_{gd}. Cappy derived an expression for the frequency at which the channel noise became frequency dependent and found it was independent of the unit gate width, for the intrinsic FET. This may still be an over simplification which the author has argued in a recent publication 2004 **[C3]** that the gate drain capacitance is dependent on the loss effects along the gate, resulting in the intrinsic value for C_{gd} being a function of the unit gate-width. This is seen as an area of further research, and could be extended to fully investigate the differences between the lumped and the distributed model of transistors with different unit-gate widths. These effects will be of significant importance to transistors fabricated on wide band gap semiconductor materials as it may be feasible to obtain low noise and with a significant power handling capability.

Theoretical modeling of the linear gate transistor (LGT) indicated to obtain the growing-wave a narrow (< 0.5 micron) gate-length with a very low resistance gate structure was required. In the mid 1980's the fabrication technology was not sufficiently mature to enable the fabrication of wide width, narrow (<0.5 micron) gate-length, low resistance gate structures. The improvements now available in fabrication technology would enable the realization of long narrow gate structures with a very low resistance. This would allow a practical travelling wave transistor supporting a growing-wave to be fabricated where the gain of the transistor is non-reciprocal and not restricted to 6 to 8 active sections, as for conventional travelling wave amplifiers. Further, the active regions of the structure could use HEMT technology to significantly improve the transconductance, and a wide-bandgap semiconductor, for example gallium nitride, opens the possibility of medium power (2 Watt) over multi-octave bandwidths. This will give a significant improvement over conventional travelling wave amplifiers fabricated on III-V materials, for example gallium arsenide, where a maximum output power of 0.1 Watt is feasible.
The author also believes that the current noise theories have not been extended to structures supporting a growing-wave. To a first approximation, Cappy [108] has shown that the minimum noise figure is dependent on the gate-width (gate/drain coupling capacitance), and if the assumption is made that the growing-wave enables the full width of the device to remain active then the minimum noise theory of Cappy perhaps can be extended to traveling transistors supporting a growing wave..

Gallium nitride is an exciting material which has only recently been synthesized with sufficient purity for the fabrication of RF and microwave HEMT devices. These devices offer numerous opportunities for future research work and some of these are summarized below:

1) Investigation of the optimum minimum noise performance of the transistor with geometry and bias conditions. Referenced work [70, **C3**] has indicated the potential of the device having a very high breakdown voltage which in some applications may preclude the requirement for a limiter in front of a low noise GaN based amplifier. This will require extensive research in-order to determine

the maximum pulsed and cw input power which can be applied before the transistor burns.

2) Some early published work on GaN devices has indicated that the saturation carrier velocity is not as sensitive to temperature when compared with GaAs [95], and when coupled with a much higher intrinsic semiconductor temperature, the GaN HEMT device may well provide a minimum noise figure performance which is less sensitive to temperature and operating to much higher temperatures than its GaAs and InP counterparts. To the authors knowledge this has not been investigated either experimentally or theoretically to any extent.

3) The saturation velocity is a figure of merit of the transistor, and for GaN it has been computed by Monte-Carlo simulation [107] and found to be approximately 2.5 times higher than for GaAs. However, the saturation velocity obtained from de-embedding from measured s-parameters has **[C1]** resulted in values of around $1.2x10^5$m/sec. Further work is required to identify whether high saturation velocities can be obtained and whether the present limiting factors are self-heating, parallel conduction and/or charge scattering due to the GaN/SiC substrate lattice mismatch. Some very recent work undertaken by Cree (Compound Semiconductor, Nov 2004) has shown a substantial improvement in the room temperature mobility by growing GaN HEMT layers directly on to a synthesised GaN substrate thereby minimising the lattice interface mismatch.

4) The GaN HEMT equivalent circuit model parameters are being mapped under all bias conditions to develop a large signal model. The work in this thesis suggests that that the access source and drain parasitic resistances vary with bias conditions which will need to be taken into account within the large signal model. Also, the experimental transconductance behavior with V_{gs} representing the GaN HEMT appears to fall off more rapidly than for a AlGaAs/GaAs HEMT and the present work has found difficulty in obtaining a good IV characteristic match with either

the Curtice-Ettenberg or the Angelov models. Further, work is required in developing improved large signal IV models for GaN transistors.

8) REFERENCES:

8.1) Published references

1) W.Shockley 'Negative resistance arising from transit time in semiconductor diodes' Bell System Tech J, 33,799, 1954.
2) W.T.Read 'A proposed high-frequency negative-resistance diode' Bell System Tech J, 37, 401, 1958.
3) J.Gunn 'Microwave oscillations of current in III-V semiconductors' IBM J1 Res.Dev.8, 141-159, 1964.
4) W.Shockley 'A Unipolar field-effect transistor' Proc I.R.E., 40, 1365-1376, Nov 1952.
5) W.Gosling et al 'Field effect electronics' Publisher Butterworth London, 1971.
6) C.A.Lee, R.L.Batdorf, W.Wiegmann, and G.Kaminsky 'The Read diode-an avalanching, transit-time negative resistance oscillator' Appl Phys. Lett. 6, 89, 1965.
7) G.Gibbons 'Avalanche-diode microwave oscillators' Clarendon Press, Oxford, 1973.
8) A.Maestraisi et al 'A planar diode frequency tripler at 1.9THz' IEEE, MTT-S, 2003, pp748 to 750.
9) H.J.Prager, K.K.N.Chang and J.Weisbrod 'High-power, high-efficiency silicon avalanche diodes at ultra-high frequencies' Proc. IEEE, 55, 586, 1968.
10) S.G.Liu '2000W –GHz complementary TRAPATT diodes' 1973 Int. Solid-State Cir.Conf. Dig of Tech papers, pp124-125.
11) C.A.Liechti 'Microwave Field-Effect Transistors-1976' IEEE, MTTS, Vol. 24, No 6, June 1976, pages 279 to 299.
12) Fujitsu Sets New Speed Record, Compound Semiconductor, Dec 2002, Volume 8, Nos. 11, page 10.
13) M.Chertuok et al 'The first 0.15 micron MHEMT 6" GaAs Foundary Service: Highly Reliable Process for 3V Drain Bias Operation' 11th GaAs Symposium Proceedings, Munich, 2003.
14) R.Pengelly 'Improving Linearity and Efficiency of RF Power Transistors for Infrastructure Applications' Wireless Design Conference, IEEE, London, May 2002.
15) Cree pushes GaN power density past 30W/mm, Compound Semiconductors, December 2003.

16) R.A.Pucel 'Some design considerations for gallium arsenide monolithic circuits' Proceedings seventh biennial Cornell conference, August 14-16th, 1979, pp 17-32.

17) M.E.Hines 'Negative resistance diode power amplification' IEEE, Trans., 1970, ED-17, pp 1-8.

18) R.Laton and G.I.Haddad, 'Characteristics of IMPATT-diode reflection amplifiers' IEEE trans. MTT-21, nos 11, Nov 1973, pp668-680.

19) A.S.Clorfeine 'Guide lines for the design of high-frequency mode avalanche diode oscillators' IEEE.trans. ED-18, 1971. pp 550.

20) W.J.Evans 'Circuits for high-efficiency avalanche diode oscillators' IEEE Trans., 1969, MTT-17, pp.1060-1067.

21) J.V.DiLorenzo and W.R.Wisseman 'GaAs power MESFETs: Design, Fabrication and Performance', IEEE, trans. MTT-27, nos 5, May 1979, pp367-378.

22) D.Z.emack et al 'High efficiency high power X-band GaAs FETs' IEDM, 1981, pp 672-675.

23) M.W.Geen, M.R.Goulding and R.M.Eaton 'The TRAPATT diode, a highly repeatable solid state microwave power generator for lw cost high volume applications' IEE, colloquium on Solid State Microwave Power Generation, 30th May 1986, digest 1986/88.

24) K.J.Russell, 'Microwave power combining techniques' IEEE Trans., 1979, MTT-27, pp. 472-478.

25) J.Turner 'Gallium Arsenide Transistors: Power at Higher Frequencies'. Systems Technology, Oct. 1981.

26) M.Shur 'GaAs devices and circuits' Plenum Press, New York, London 1987.

27) P.Roblin and H.Rohdin 'High-speed heterostructure devices' Cambridge University Press, published 2002.

28) R.S.Pengelly 'GaAs Monolithic Microwave Integrated Circuits-Their impact on future systems' A.C.R.C. Ann. Rev. pp 69 – 80, 1984.

29) P.Solomon, H.Morkoc 'Modulation-doped GaAs/AlGaAs heterojunction field –effect transistors (MODFETs), ultrahigh speed devices for supercomputers' IEEE trans ED-31, nos 8 August 1984, pp 1015-1027.

30) Serge Luryi et al 'Charge Injection Transistor based on real-space Hot-Electron Transfer' IEEE, trans ED31, nos 6, Jiune 1984, 832-839.

31) K.Hirakawa, H.Sakaki, and J.Yoshino 'Mobility modulation of the two-dimensional electron gas via controlled deformation of the electron wave function in selectively doped AlGaAs-GaAs heterojunctions' Physical Review Letters, vol 54, nos 12, 25th March 1985, pp 1279-1282

32) A.S.Podgorski and L.Y.Wei 'Theory of traveling wave transistors' IEEE trans ED-29, 1982, pp1845-1853.

33) M.Feng et al 'Temperature dependent study of the microwave performance of 0.25 micron gate GaAs MESFET's and GaAs Pseudomorphic HEMT's' IEEE trans. ED-43, nos 6, July 1996, pp 852-860.

34) R.I.Taylor and A.J.Holden 'Modelling the noise properties of pseudomorphic HEMTs' Electronic Letters, 1993.

35) C.H.Oxley 'Active devices suitable for milli-metric wave operation' IEE Colloquium, 1986.

36) N.Tanahashi, 'A wide-band ultra low noise amplifier mmic using GaAs Phemt', IEEE, MTTS, 2003, pp2225-2228.

37) N.A.Slaymaker and J.Turner 'Microwave FET amplifiers with centre frequencies between 1 and 11 GHz' Proc EMC, Vol 1, 1973.

38) D.Daniel, P.Forrest, R.H.Bennett, C.H.Oxley, annual research report, 'GaAs FETs at Frequencies above 20GHz' RP9342, Nov '81 to Oct'82.

39) D.R.Brambley and R.H.Bennett 'Electron Beam Lithography' A.C.R.C. Ann. Rev,

40) J.Arnold, P.Forrest, D.Daniel, R.Bennett and C.H.Oxley 'HF GaAs FET Amplifiers' IEE Colloquium, London, Dec 1982.

41) S.H.Wemple et al 'Control of gate-drain avalanche in GaAs MESFETs' IEEE trans ED-27, 1980, pp1015-1018.

42) W. Liu 'Fundamentals of III-V Devices HBTs, MESFETs and HFETs/HEMTs' John Wiley and Sons, inc. 1999.

43) C.H.Oxley, I.Davies, S.Cotton and D.Brambley, Final Research Report 'GaAs FETs at frequencies above 20GHz', Plessy Co, RP9234, March 1986.

44) A.Phillips 'Summary of wide bandgap microwave power devices', RF2001, Workshop Proceedings, Cambridge, 2nd April 2001.

45) R.Pengelly 'Amplifiers' Microwave Subsystem Design, Leeds Summer School, 1987, pp241-305.

46) R.A.Pucel, H.A.Hans and H.Statz 'Signal and noise properties of gallium arsenide microwave field-effect transistors' Advances in Electronics and Electron Physics' Vol.38, NY, Academic Press pp195-265.

47) I.Davies, R.H.Bennett and C.H.Oxley, Annual Research Report,'GaAs FETs at frequencies above 20GHz' RP9234, Nov t0 Oct 1983.

48) H.Fukui 'Optimum noise figure of microwave GaAs MESFETs' IEEE Trans, ED-26, 7, 1979, pp 1032-1037.

49) Onodera Kiyomitsu, Nishimura Kazumi, Aoyama Shinji, Sugitani Suehiro, Yamane Yasuro, and Hirano Mayoto ' Extremely Low-Noise Performance of GaAs MESFET's with Wide-Head T-Shaped Gate' IEEE Trans ED, vol 46, No 2, February 1999.

50) W.Patrick, W.S.Mackie, S.P.Beaumont, C.D.W.Wilkinson and C.H.Oxley 'Very Short Gate-Length GaAs MESFET's', IEEE Electron Device Letters, Vol. EDL-6, No.9, September 1985.

51) P.Ladbrooke 'MMIC design:GaAs FETs and HEMTs' Norwood, MA: Artech House, 1989.

52) C.Wolfe, N.Holonyak, and G.Stillman 'Physical properties of semiconductors', Prentice Hall, Englewood Cliffs, New Jersey, 1989.

53) P.Hower and G.Brechtel , IEEE trans. ED-20, nos 3, pp 213-220.

54) John Walker 'High power GaAs FET amplifiers' publisher Artech, 1993.

55) G.Dambrine, A.Cappy, F.Heliodore and E.Playez 'A new method for determining the FET small-signal equivalent circuit', IEEE Trans. Microwave Theory and Tech., vol 36, pp1151-1161, 1988.

56) S. Pritchett, A. Fernandez, D. Bridges and K. Whelan 'Improved FET Noise Extraction Method for Statistical Model Development' IEEE, MTTS- Digest, 1995, pp 943-946.

57) H.Fukui 'Optimum noise figure of microwave GaAs MESFETs', IEEE Trans., 1979, ED-26, (7), PP. 1032-1037.

58) R.A.Purcel, H.A.Haus, and H.Statz 'Signal and noise properties of gallium arsenide microwave field-effect transistors', Advances in Electronics and Electron Physics, vol 38, Academic Press, New York, 1975, pp 195-265.

59) W.C.Bruncke and A.Van der Ziel 'Thermal noise in junction-gate field effect transistors', IEEE trans. ED-13, March 1966, pp 323-329.

60) A.Podell 'A functional GaAs FET noise model' IEEE trans. ED-28, nos 5, May 1981, pp 511-516.

61) D. Delagebeaudeuf, J. Chevrier, M. Laviron, P.A.Delescluse 'Anew relationship between the Fukui coefficient and optimum current value for low noise operation of fiel-effect transistors' IEEE ED Lett 1985; EDL-6(9), pp 444-445.

62) W.Lu etal 'AlGaN/GaN HEMTs on SiC with over 100GHz ft and low microwave noise' IEEE Trans ED, vol. 48, 2001, pp581-585.

63) Lu W, Kumar V, Piner E, Adesida I "DC, RF, and microwave noise performance of AlGaN/GaN field effect transistors dependence of aluminum concentration", IEEE Trans Electron Devices, April 2003.

64) T.Itoh and R.Mittra 'Spectral domain approach for calculating the dispersion characteristics of microstrip lines' IEEE Trans. MTT, July 1973

65) W.Getsinger 'Microstrip dispersion model' IEEE Trans, MTT January 1973.

66) Mirshekar-Syankal. D and Davies. J. B 'Accurate solution of microstrip and coplanar structures for dispersion and for dielectric and conductor losses' IEEE MTT, vol. 27, pp 694-699, July 1979.

67) C.H.Oxley '30 GHz low noise GaAs FET amplifier' Phase 1, ESTEC 4490/80/NL/MS. 1984.

68) C.Liechti 'Micowave Field –Effect Transistor –1976' IEEE Trans MTT-24, nos 6, June 1976.

69) W.Lu, V.Kumar, E.Piner and I.Adesida 'DC, RF, and microwave noise performance of AlGaN/GaN Field Effect Transistors dependence of Aluminum Concentration' IEEE, ED April, 2003.

70) N.X.Nguyen et al 'Robust low microwave noise GaN MODFETs with 0.6dB noise figure at 10GHz' Electronic Letters, vol 45, June 2001, pp 677-682.

71) The Microwave Handbook vol1, Microwave components, Chapman and Hall, 1993.

72) W.RFrensley and H.M.Macksey 'Effect of gate stripe width on the Gain of GaAs MESFETs', Proceedings, Seventh Biennial Cornell Conference, August 14 to 16th, 1979, pp445-452.

73) J.Arnold and C.H.Oxley 'High gain temperature compensated EHP GaAs MESFET amplifier' Proceedings EMC, April 1984.

74) E.L.Grinzton et al, 'Distributed Amplification' Proc IRE, vol 36, 1984, pp 956-969.

75) J.Pusl, B. Agarwal, R. Pullela, L .D. Nguyen, M. V. Le, M J.W. Rodwell, L. Larson, J. F. Jensen, R. Y. Yu and M. G. Case 'Capacitive-Division Travelling-Wave Amplifier with 340GH_z Gain-Bandwidth Product' IEEE MTTS Digest 1995, pp 1661-1664.

76) W.Jutzi 'MESFET distributed amplifier with 2GHz bandwidth' Proc IEEE, vol 57, 1969, ppl195-1196.

77) E.W.Strid and K.R.Gleeson 'A DC-12GHz monolithic GaAs FET distributed amplifier' IEEE, trans. MTT, vol 30, 1982, pp969-975.

78) Y.Ayasli et al 'A monolithic GaAs 1 to 13GHz, traveling-wave amplifier', IEEE trans.MTT, vol 30, 1982, pp 976-981.

79) A.S.Podgorsk et al 'Theory of traveling wave transistors' IEEE trans. ED, vol 29, 1982, pp 1845-1853.

80) M. Farina, L. Pierantoni, and T. Rozzi 'Field Analysis and Design Criteria for T-Gate TW-FET's with Positive Gain' IEEE, MTT-S Digest 1995, pp 1269- 1272.

81) Y.Ayasli 'Decade bandwidth amplification at microwave frequencies' Microwave Journal, April 1984, pp 71-79.

82) Y.Ayasli et al 'Monolithic 2 to 20GHz GaAs traveling-wave amplifier' Electronics Letters, vol 18, 8th July, 1982.

83) C.Nishimoto et al 'A 2-20GHz, high gain, monolithic HEMT distributed amplifier' IEEE MTT-S Digest, 1987, pp 155 – 158.

84) A.C.Weitz 'RF power devices for wireless communication' MTTS Proceedings, 2002, pp285-288.

85) S.Lee et al 'Demonstration of a high efficiency nonuniform monolithic gallium nitride distributed amplifier' IEEE, MTT-S, 2000, pp1-4.

86) L.F.Eastman et al 'Undoped AlGaN/GaN HEMTs for Microwave Power Amplification' IEEE Trans Elec Dev, vol. 48, pp 479-485, 2001.

87) J.Suresh, M.Willander and R.Van Overstraeten 'Compound semiconductors strained layers and devices' Academic publishers, 2000.

88) L.Eastman 'GaN reaches new power levels' Compound semiconductor, Nov 2001, vol 7, nos 10.

89) S.C.Jain etal 'III-Nitrides: Growth, characterization and properties' Applied Physics Reviews, JOAP, vol 87, Nos 3, 2000, pp 965-1005.

90) N.X.Nguyen, M.Micovie, W.S.Wong, P.Hashimoto, J.Janke,D.Harvey, C.Nguyen 'Rhobust low microwave noise GaN MODFETs with 0.6dB noise figure at 10GHz', Electronic Lett., vol 36, pp 469-471, 2000.

91) J.M.Golio 'Microwave MESFETs and HEMTs' Artech House, 1991.

92) M.J.Uren et al 'Back bias effects in AlGaN/GaN HFETs' Phys.stat.sol, 2002, pp 1-4.

93) F.Ren and J.C.Zolper 'Wide energy bandgap electronic devices' World Scientific, 2003.

94) A.T.Ping etal 'Microwave noise performance of AlGaN/GaN HEMTs' Electronic Letters, 2000, online paper 20000152.

95) M.Wraback et al 'Measurement of transit time and carrier velocity under high electron field in III-Nitride PIN diodes' Materials Research Society Symposium Proceedings, vol. 622, April 2000.

96) V.Kumar, W.Lu, R.Schwindt, A.Kuliev, G.Simin, J.Yang, M.A.Khan, and I. Adesida 'AlGaN/GaN HEMTs on SiC with f_t of over 120GHz' IEEE Electron Device Letters, vol 23, pp 455-457, 2002.

97) H.M.Ng et al 'The role of dislocation scattering in n-type GaN films' Applied Physics Letters, vol 73, nos 6, 10th August 1998, pp 821-823.

98) P.Nevermann 'Simulation of temperature dependencies using a new CAD suitable physical GaAs model, including the electron pre-heating effect' IEEE, MTTS, 1995, pp 931-934.

99) L.F.Eastman et al 'Undoped AlGaN/GaN HEMTs for microwave power amplification' IEEE trans.ED-48, 2001, pp479-485.

100) W.Lu, J.Yang, M.A.Khan and I.Adesida 'AlGaN/GaN HEMTs on SiC with over 100GHz ft and low microwave noise' IEEE Trans ED, March 2001, volume 48, nos 3, pp 581-586.

101) R.J.Trew 'AlGaN/GaN HFET amplifier performance and limitations' IEEE, MTT-S, 2002, pp 1811-1814

102) S.Jain et al 'Compound semiconductors strained layers and devices' Kluwer academic publishers, 2000.

103) R.S.Balmer et al 'AlGaN/GaN microwave HFET including a thin AlN carrier exclusion layer' Physics.stat.sol, 2003, pages 1 to 4.

104) L.Ardaravicius et al 'Electron drift velocity in AlGaN/GaN' Applied Physics Letters, vol 83, 2003, pp 4038-4041.

105) Sungjae Lee et al 'Intrinsic noise characteristics of AlGaN/GaN HEMTs', MTT-S, 2002, pp1415-1418.

106) D.S.Shin et al 'Analytical noise model with the influence of shot noise induced by the gate-leakage current for submicrometer gate-length high electron mobility transistors' IEEE trans ED, vol 44, nos 11, Nov 1997, pp 1883-1887.

107) U.V. Bhadkar and M.S.Shur 'Monte Carlo calculation of the velocity-field characteristic of Wurtzite GaN' J.Appl Phys, 1997, vol 82(4), pp1649 -1655.

108) A.Cappy 'Noise modeling and measurement techniques' IEEE trans MTT, 1988, 36(1), pp 1-10.

8.2) Industrial/MOD/INTEL/ESA internal reports

1) X-band silicon TRAPATT oscillator RP9-133, Final Research Report, Nov 1974 to Sept 1975.
2) X-band TRAPATT amplifier module VX9399, Interim Report phase 1, Oct 1975 to May 1976.
3) X-band TRAPATT amplifier module VX9399, Final Technical Report/phase 3, March1977-March 1978.
4) J-band IMPATT amplifier, VX9432, Final Technical Report, March 1980.
5) GaAs FETs at frequencies above 20GHz, RP9-234, Annual Research Report, Nov 1981-Oct 1982.
6) GaAs FETs at frequencies above 20GHz, RP9-234, Annual Research Report, Nov 1982-Oct 1983.
7) GaAs FETs at frequencies above 20GHz, RP9-234, Annual Research Report, Nov 1983-Oct 1984.
8) GaAs FETs at frequencies above 20GHz, RP9-234, Final Research Report, March 1986.
9) Study of a travelling wave GaAs FET, RP9-262, Annual Research Report, Nov 1981-Oct 1982.
10) Study of a traveling wave GaAs FET, RP9-262, Annual Research Report, Nov 1982-Oct 1983.
11) Study of a travelling wave GaAs FET, RP9-262, Annual Research Report, Nov 1983-Oct 1984.
12) Study of a travelling wave GaAs FET, RP9-262, Annual Research Report, March 1985.
13) Microwave monolithic and impedance matched GaAs power FETs, RP9-261, Final Report, March 1986.
14) Proposal INTEL-345, February 1983, Travelling Wave III-V semiconductor MESFETs.
15) INTEL-345, Travelling wave III-V semiconductor Devices, 1st Quarterly Progress Report, 14th Nov 1983 to 14th February 1984.

16) INTEL-345, Travelling wave III-V semiconductor Devices, 2nd Quarterly Progress Report, 14th Feb 1984 to 14th May 1984.

17) INTEL-345, Travelling wave III-V semiconductor Devices, 3rd Quarterly Progress Report, 14th May 1984 to 14th September 1984.

18) INTEL-345, Travelling wave III-V semiconductor MESFETs, Final Report, January 1986.

19) INTEL-173, Low noise gallium arsenide FET for ISL application, Final Report, July 1985.

20) 30GHz low noise GaAs fet amplifiers, ESA 4490/80/NL/MS, Final Report, Sept 1984.

21) Proposal ESA (711B/6704), 20GHz LNA for

22) Ku-band Read Diode Development for Matra, Report nos 181/87/111, December 1987.

23) GaAs millimetric wave transistors and integrated circuits, February 1986, Response to IEPG TA-1, RFP1.

24) INTEL-173,Low noise gallium arsenide FET for ISL application, Proposal, 1981.

APPENDIX 1: CITATIONS FOR SECTION A

Citation list

Citation search engines (Web of science and IEEE) appear not to cover 1972-1982.

APPENDIX 2: CITATIONS FOR SECTION B

Citation list

Publication **B2**

1) Benhabiles MT, Benghalia A, Lassoued S 'Traveling-wave dual gate MESFET: A multimode S-matrix derivation based on the quasistatic approach' INT J RF MICROW C E 8 (1): 11-19 Jan 1998.
2) Ongareau E, Aubourg M, Obregon JJ 'A nonlinear and distributed modelling procedure of FETs' INT J NUMER MODEL EL 6 (4): 309-319 Sept-Oct 1994.
3) Ongareau E, Bosisio RG, Aubourg M 'A nonlinear and distributed modelling procedure of FETs' INT J NUMER MODEL EL 6 (4): 237-251 Nov 1993.
4) Hickson MT, Gardner P, Paul DK 'A semidistributed hemt model for accurate fitting and extrapolation of s-parameters and noise parameters' IEEE T MICROW THEORY 40 (8): 1709-1712 Aug 1992.
5) Pospieszalski MW 'Modeling of noise parameters of MESFET and MODFET and their frequency and temperature –dependence' IEEE T MICROW THEORY 37 (9): 1340-1350 Sept 1989.
6) Heinrich W 'High frequency MESFET noise modelling including distributed effects ' IEEE T MICROW THEORY 37 (5): 836-842 May 1989.
7) Ghione G, Naldi CU, Filicori F 'Physical modeling of GaAs MESFETs in an integrated CAD envvironment from device technology to microwave circuit performance' IEEE T MICROW THEORY 37 (3): 457-468 Mar 1989.

Publication **B3**

1) Gupta MS, Pitzalis O, Rosenbauum SE 'Microwave noise characterisation of GaAs MESFETs- evaluation by on wafer low frequency output noise measurement' IEEE T MICROW THEORY 35 (12): 1208-1218 Dec 1987.

Publication **B5**

1) Sitch JE 'Microwave Semiconductor devices' REP PROG PHYS 48 (3): 277-326 1985.

Publication **B7**

1) M.Shur. 'GaAs Devices and Circuits' Plenum Press, New York, London, 1987.
2) P.W.Chyne and C.Huang 'Quarter micron low noise GaAs FETs' IEEE Electron Devices, 1983.

Publication **B8**

1) Jastrzebski AK, 'Non-linear MESFET modelling' Proc EMC 17, 7-11th Sept 1987, pages 599-604.

Publication **B12**

1) Narahara K, Otsuji 'Characterisation of wave propagation on traveling-wave field effect transistors' JPN J APPL PHYS 1 37(12A): 6328-6339 Dec 1998.
2) Farina M, Morini A, Pierantoni L 'Eletromagnetic investigation on the propagation in distributed active devices' IEE P-MICROW ANTEN P 144(5): 281-288 Oct 1997.
3) Benhabiles M.T, Benghalia A, Lassoued S 'Traveling-wave dual-gate MESFET: A multimode s-matrix derivation based on the quasistatic approach' INT J RF MICROW CE8 (1): 11-19 Jan 1998.
4) Abdipour A, Pacaud A 'Complete sliced model of microwave FETs and comparison with lumped model and experimental results' IEEE T MICROW THEORY 44 (1): 4-9 Jan 1996.
5) Bosey V, Rapoport Y, Senchenko V, 'FET model taking into account wave characterisation of the active-region and input circuits' IEEE T MICROW THEORY 43 (7): 1453-1460 Jul 1995.
6) IEEE MTT-S May 16-20, 1995, Vol3, pp 1269-1272.
7) Anand MB, Ghosh PK, Kornreich PG ' A travelling-wave high-electron mobility transistor' IEEE T MICROW THEORY 41 (4): 624-631 Apr 1993.
8) Dagostino S, Dinzeo G, Tudini L ' Analytical modeling and design criteria for travelling-wave FET amplifiers' IEEE T MICROW THEORY 40 (2): 202-208 Feb 1992.
9) Rauschenbach K, Lee CA 'Design and fabrication of the self-aligned opposed gate source transistor' IEEE T ED 39 (2): 219-225, Feb 1992.

10) Shire D, Jackson T, Tasker P 'Characterisation of travelling-wave MODFETs by electroopic sampling' INST PHYS CONF SER (96): 471-474 1989.

11) Han K, Wong TTY 'Coupled-wave small-signal transient analysis of GaAs distributed-amplifier' IEEE T MICROW THEORY 38 (1): 23-29 Jan 1990.

12) Electronics Letters 16th March 1989, Vol25, No. 6, pp 403-404.

13) Elghazaly SM, Itoh T, 'Travelling-wave inverted-gate field effect transistors-concept, analysis and potential' IEEE T MICROW THEORY 37 (6): 1027-1032 Jun 1989.

14) Fricke K 'Measurement of the distributed properties of GaAs –MESFETs' INT J ELECTRON 65 (4): 769-777 OCT 1988.

15) Elghazaly S, Itoh T 'Inverted-gate field-effect transistors –novel high-frequency structures' IEEE ED 35 (7): 810-817 Part 1 Jul 1988.

16) Lippens D, Friscourt MR, Rolland PA 'Solid-state power devices in the millimeter-wave range' REV PHYS APPL 22 (11): 1433-1450 Nov 1987.

17) Hsieh HC, 'Coupled mode theory in a lossy, nonlinear transmission-line system' J APPL PHYS 62 (5): 2095-2102 Sept 1 1987.

18) Heinrich W 'Distributed equivalent-circuit model for travelling-wave FET design' IEEE T MICROW THEORY 35 (5): 487-491 May 1987.

19) Fricke K, Hartnaagel HL, Tiwari DC 'High-efficiency frequency doubling by GaAs travelling wave MESFETs' IEEE T ED 34 (4): 742-745 Apr 1987.

20) Heinrich W, Hartnagel HL 'Wave-Propagation on MESFET electrodes and its influence on transistor gain' IEEE T MICROW THEORY 35 (1): 1-8 Jan 1987.

21) Holden AJ, Eddison CG, Metcalfe JG 'Bipolar heterojunction transistor integrated – circuits design modeling and characterisation' Electron Lett. 22 (15): 815-816 Jul 17 1986.

22) Tiwaari DC, Hartnagel HL 'Nonlinear coupled transmission-line analysis for 2nd harmonic generation in travelling wave GaAs MESFETs' IEEE T ED 33 (3): 366-372 Mar 1986.

APPENDIX 3: CITATIONS FOR SECTION C

CITATION LIST

Publication **C3**

1) Johnson JW, Ren F, Pearton SK 'Performance of AlGaN/GaN high electron mobility transistors at nanoscale gate lengths' J NANOSCI NANOTECHNO 2 (3-4):325-332 Jun-Aug 2002.
2) Lue B, Johnson JW, Kim J 'Influence of MgO and Sc203 passivation on AlGaN/GaN high electron mobility transistors' APPL PHYS LETT 80 (9): 1661-1663 Mar 4 2002.
3) Lu W, Kumar V, Piner E and Adesida I 'DC,RF, and microwave noise performance of AlGaN/GaN Field Effect Transistors Dependence of Aluminium Concentration' trans IEEE ED, April: 2003

APPENDIX 4

Letter from Dr. A. J Holden confirming originality of the presented work:

15, Octavian Way,
Brackley, Northamptonshire,
NN13 7HX.
Telephone: 01280 703769(Home)
07720 344797(Mbl.)
e-mail: t.holden@physics.org

Date: 28th March 2004

To whom it may concern

Dear Sirs,

Re: **SOLID-STATE MICROWAVE AMPLIFICATION INTO MILLIMETRIC FREQUENCIES for consideration of PhD by published works - submitted by Mr. C.H. Oxley – April 2004.**

I write in order to endorse this thesis, confirm the originality of the material and emphasise the innovative and independent nature of the work performed by Mr. Oxley, particularly in areas where we collaborated and produced co-authored publications.

My direct involvement with Mr. Oxley's research was in his second period in the 1980s when he was developing state of the art GaAs transistors for microwave and millimetre wave applications. I have, however been actively aware of his research throughout the whole period reported. During the 1980s Mr. Oxley was Device Engineer with design authority for the research devices we were working on at Caswell. My role was as Device Physicist responsible for device modelling and analysis. As detailed in the thesis Mr. Oxley undertook the device design, fabrication and characterisation and mastered the challenges of making the technology work in these advanced structures. In turn his work provided parameters to feed my modelling activity and enabled us to iterate the design. He was also responsible for the development of the noise analysis and the analysis and understanding of the overall RF performance of the devices.

As explained in the thesis, these devices were required to perform at and beyond the capability of the GaAs device technology available at the time. This was particularly true of the travelling wave structures such as the Linear Gate Transistor and Mr. Oxley was

instrumental in pushing the boundaries of the technology and achieving world beating results in what was a very exciting era for GaAs research.

I have read through the thesis and am satisfied that, in the areas where I was involved in the work in the 1980s, the research described is directly attributable to Mr. Oxley and demonstrates the outstanding contribution he made to the subject in that period. He has made appropriate and accurate reference to other work and contributions where he has relied on collaboration and inputs from other sources.

It has been a pleasure and a privilege to work with Mr. Oxley and I commend his work very highly. The research described covers a long and exciting period in III-V device technology and represents an original and valuable contribution to that development.

Yours faithfully,

Dr. A.J. Holden BSc. PhD (Cantab), CPhys. M.Inst.P.

Dr. Holden is a Solid State Physicist with interests in semiconductor microwave and optoelectronic devices, electronic materials, sensors and nanotechnology. Educated at Manchester and Cambridge Universities, he has worked on research and development in a variety of industrial roles for Plessey, GEC, Marconi and Bookham Technology. He is currently a consultant physicist working on new materials and device concepts for next generation technologies. He works widely with Universities in the UK and abroad through EPSRC, European and bilateral collaborations, is a referee for the EPSRC and a number of leading scientific journals and has acted regularly as an external referee for PhD theses.

APPENDIX 5

C.H.Oxley & A.J.Holden 'Travelling-wave field-effect transistor patent GB2156152A

(12) UK Patent Application (19) GB (11) 2 156 152 A

(43) Application published 2 Oct 1985

(21) Application No 8506557

(22) Date of filing 13 Mar 1985

(30) Priority data
(31) 8407275 (32) 21 Mar 1984 (33) GB

(51) INT CL*
H01L 29/80

(52) Domestic classification
H1K 1CB 4C1M 4C1R 4C1U 4C2U 9B1 9B1A CB

(56) Documents cited
None

(58) Field of search
H1K

(71) Applicant
The Plessey Company plc (United Kingdom),
Vicarage Lane, Ilford, Essex

(72) Inventors
Christopher Hunter Oxley
Anthony James Holden

(74) Agent and/or Address for Service
H J Field,
The Plessey Company plc, Vicarage Lane, Ilford, Essex

(54) **Travelling-wave field-effect transistor**

(57) In a transistor having on a semiconductor substrate (10) continuous elongate source (30), drain (40) and gate (50) electrodes, gain is improved by dividing the structure into active and passive sites and by providing inductive coupling to supply power feedback to the gate electrode and thereby to sustain and enhance guided wave propagation. The drain electrode (40) has a meander configuration to provide inductive coupling to the gate electrode and balance the waves on drain and gate (50). At each active site, protrusions (32,34,36) extend from the source electrode (30), and protrusions (42,44,46) extend from the drain electrode (40). The parasitic capacitance at each passive site is thus minimised. The source and drain protrusions are connected by channels (22) in the underlying semiconductor substrate (10,16) and the conductivity of these channels (22) controlled by gate operation. To reduce resistive losses, the gate electrode (5) is of larger cross-section at passive sites. Also the gate electrode (50) is of T-section shape at each active site.

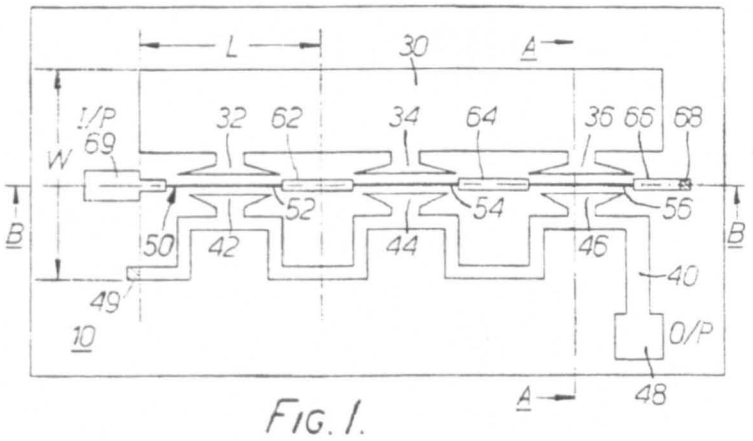


FIG. 1.

GB 2 156 152 A

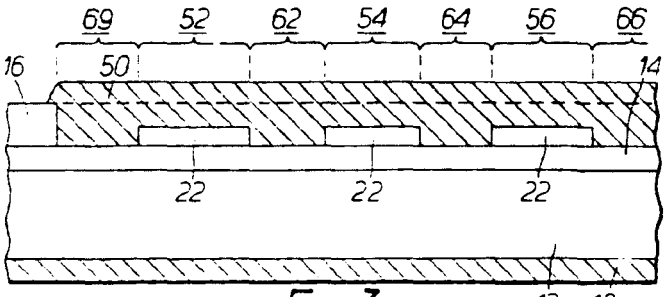


FIG. 3.

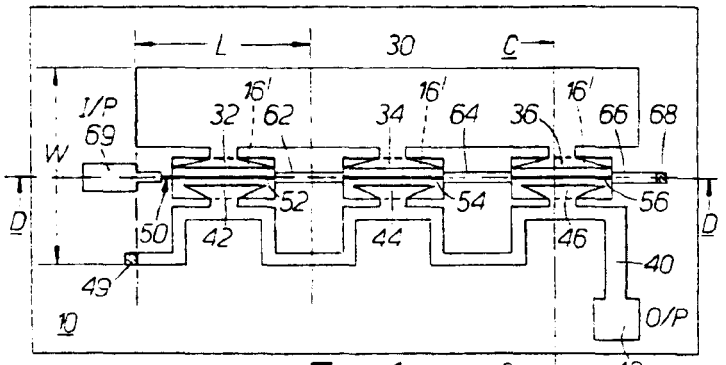


FIG. 4.

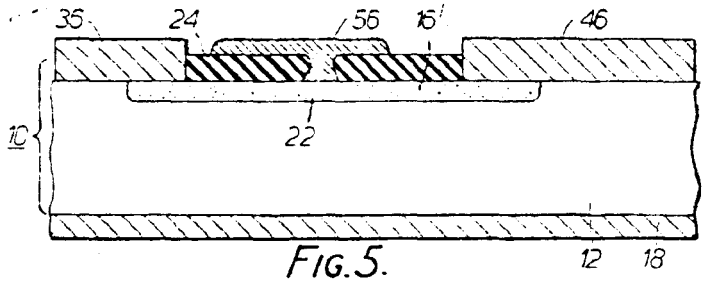


FIG. 5.

SPECIFICATION

Improvements in or relating to transistors

The present invention relates to transistors, particularly travelling-wave field-effect transistors.

A typical travelling-wave field-effect transistor comprises three continuous elongate parallel electrodes, namely a source electrode, a gate electrode and a drain electrode, adjacent to a layer of semiconductor material, this layer providing a common channel between the source and drain electrodes. In this construction a travelling-wave is generated and velocity coherence is maintained by means of distributed lumped capacitance. This latter is provided by a dielectric overlay and lateral conductors spaced apart along the length of the device, each being grounded by contact to the source electrode. Use of complex balun circuits is also typical and adds to the design complexity.

The present invention is intended to provide a travelling-wave field-effect transistor of simpler construction and, for a given gate width, one exhibiting an enhanced gain.

According to this invention there is thus provided a travelling-wave field-effect transistor comprising:

a supportive substrate of semiconductor material;

a continuous elongate source electrode,

a continuous elongate gate electrode, and

a continuous elongate drain electrode; and

including,

a plurality of lateral conductive channels underlying and spaced apart along the length of the gate electrode and extending between the source and drain electrodes, defining thus a plurality of distributed active sites, and

inductive coupling between the drain and gate electrodes, to provide feedback to sustain and enhance wave propagation.

Conveniently, the inductive coupling aforementioned may be provided by meander configuration of the drain electrode. The feedback of power from the drain electrode to the gate electrode compensates for loss in the gate electrode and assists in the generation of a growing wave. The longer drain line also balances the wave velocities on the drain and gate lines.

Preferably, the source electrode, or the drain electrode, or both, are provided with protruding portions, one at each active site. The consequent wider spacing of electrodes thus permitted at the passive sites results in reduction of parasitic capacitance effects.

It is advantageous to configure the gate electrode to have greater cross-section area at the passive sites. This allows reduction of resistive losses along the gate electrode.

It is furthermore advantageous to configure the gate electrode to be of T shaped cross-section at the active sites. This affords a thin region for gate operation, whilst at the same time providing a wider region to enhance conduction. It is preferable that this wider region is offset laterally relative to the thin region to lie closer to the source electrode. This latter construction has the advantage of improved breakdown characteristics.

Embodiments of this invention will now be described, by way of example only, and with reference to the accompanying drawings in which:—

Figure 1 is an outline plan view of a travelling-wave field-effect transistor constructed in accordance with this invention, and showing electrode configuration;

Figure 2 is an expanded cross-section view of this transistor, taken along the section A–A of Fig. 1;

Figure 3 is another cross-section view of this transistor, taken along the section B–B of Fig. 1;

Figure 4 is an outline plan view of a travelling-wave field-effect transistor, also constructed in accordance with this invention, a variant of the transistor shown in the preceding Figures; and

Figure 5 is an expanded cross-section view of this latter transistor, taken along section C–C of Fig. 4.

With reference to Figs. 1 to 3, there is shown a travelling-wave field-effect transistor. This comprises a composite semiconductor substrate 10 formed of a base substrate 12, a buffer layer 14 and an active layer 16. In this example the substrate 10 is of homogenous composition, but hybrid construction is not precluded and the buffer layer 14 can be of, for example, superlattice structure. A backing electrode metallisation 18 is formed on the underside of the base substrate 12. A groove 20 is defined along the length of the device. This groove 20 is configured so that at spaced intervals the groove is shallow. A channel 22 in the active layer 16 is thus left beneath the groove 20 at each of these sites. Elsewhere, the groove 20 is deeper and extends down to the buffer layer 14. The walls of the groove 20 and the upper surface of the active layer 16 adjacent to this groove 20 are coated with insulator material 24.

A continuous elongate source electrode 30 is formed on the surface of the active layer 16, and runs parallel to the groove 20. At spaced intervals along the length of this electrode 30, protruding regions 32, 34 and 36 are provided. These are located at positions corresponding to the shallow groove sites.

A continuous elongate drain electrode 40 is formed on the surface of the active layer 16 on the opposite side of the groove 20. This also extends in a direction parallel to the groove 20 and is provided with protruding regions 42, 44 and 46. These also are located at positions corresponding to the shallow

groove sites and lie opposite the protrusions 32,34 and 36 of the source electrode 30. The protrusions 32,34,36,42,44 and 46 are shown as triangular in shape, but other shapes are not precluded. The drain electrode 40 is provided with an output termination 48, and a terminating impedance 49 at its front end.

A continuous elongate gate electrode 50 is provided between the source and drain electrodes 30,40. This is formed by metal deposited over the groove 20 and the insulating coating 24. Schottky contact gates 52,54 and 56 are formed, one at each shallow groove site, at the interface between this metal and the active layer 16 at the base of the groove 20. At these sites the cross-section of the gate electrode 50 is T-shaped. The vertical portion of the T defines a thin active stripe for controlling the conductivity of the underlying channel 22, whilst the horizontal portion of the T permits enhanced conduction along the gate electrode 50, thus reducing resistive losses At other regions 62,64 and 66 of the gate electrode 50, the cross-section is wider and deeper—allowing yet further enhancement of conduction along the gate electrode 50. This gate electrode 50 is provided with a terminating impedance 68 and an input terminal 60.

It will be noted that the drain electrode 50 has a meander configuration. This is to provide inductive coupling between the drain electrode 40 and the gate electrode 50. It has been designed so that power feedback provided, from the drain electrode 40 to the gate electrode 50, sustains and enhances wave propagation along the device. The meander also balances the wave velocities on the drain and gate transmission lines.

The transistor described above thus comprises a plurality of distributed active sites. Each of thee sites includes: a source region 32,34,36; a gate 52,54,56; and, a drain region 42,44,46. Channels 22 provide a controlled conduction path for carriers between each of the source regions and the corresponding drain regions, at each of these active sites.

In the foregoing example the substrate 10 is of III–V semiconductor material, gallium arsenide. Typical resistivity values for the base substrate material 12 and the buffer layer 14 are 10^6–10^7 ohm.cm and 10^{12}–10^{13} ohm.cm respectively. The active layer is a vapour phase epitaxially grown layer of n-type gallium arsenide. This includes between 0.1 and 10×10^{17} atoms/cc of donor dopant, either High dopant concentration being chosen for low noise performance, or a high dopant concentration being chosen for power performance.

Typical dimensions for the above transistor are given as follows:—

Repeat pattern length L (Fig. 1): 50 microns to 1.0mm.

Pattern width W (Fig. 1): 0.2 to 5.0mm

Minor gate length L' (Fig. 2): 0.15 to 1 microns.

Major gate length L'' (Fig. 2): 1.0 to 5. microns.

The gate electrode 50 may be of high conductivity alloy, for example one of the titanium alloys: titanium aluminium, titanium nickel gold, titanium platinum gold, or titanium tungsten gold.

The source and drain electrodes 30, each formed from an ohmic contact in contact with the III–V semiconductor layer 16 and have a thick metallisation contact—preferably gold on top.

In the variant construction shown in Figs. 4 and 5, the source, gate and drain electrodes 30 50 and 40 are of planar construction and are supported directly on a base substrate. Active regions 16', which provide the conductive channels 22, are defined in the substrate 12 by ion implantation.

A further distinguishing feature of this variant is the form of the gate electrode 50. In this example the upper extremity of the gate section is offset relative to the lower extremity. It is offset so that the upper extremity lies closer to the source electrode 30 and further from the drain electrode 40. (The gate electrode 50, shown in Fig. 1, may also be offset in this manner.) Typical spacings between source and gate electrodes, and between gate and drain electrodes are in the case 2 and 4 microns, respectively.

CLAIMS

1. A travelling-wave field-effect transistor comprising —

a supportive substrate of semiconductor material;

a continuous elongate source electrode;

a continuous elongate gate electrode; and

a continuous elongate drain electrode; and including a plurality of lateral conductive channels underlying and spaced apart along the length of the gate electrode and extending between the source and drain electrodes defining thus a plurality of distributed active sites, and inductive coupling between the drain and gate electrodes, to provide feedback to sustain and enhance wave propagation.

2. A transistor, as claimed in claim 1, wherein the drain electrode is of a meander configuration and provides the inductive coupling as aforesaid and balances the wave velocities on the drain and gate transmission lines.

3. A transistor, as claimed in either of claims 1 or 2, wherein the source electrode, the drain electrode, or both, have protrudings, one at each active site.

4. A transistor, as claimed in any one of the preceding claims, wherein the gate electrode is of greater cross-section at passive sites, ie. at sites between the active sites as aforesaid.

5. A transistor, as claimed in any the preceding claims wherein the gate electrode is of T-section shape at each of its active sites.

6. A transistor, as claimed in claim wherein the upper extremity of each is offset relative to its lower extremity upper extremity of the gate electrode closer to the source electrode than to drain electrode.

7. A transistor, as claimed in any the preceding claims, wherein the substrate of III–V semiconductor material, the aforesaid extending beneath the base groove in this substrate and being composed of epitaxially grown material.

8. A transistor, as claimed in any the preceding claims 1 to 6, the substrate having ion implanted regions, which provide the channels aforesaid.

9. A travelling-wave field-effect transistor constructed, adapted and arranged to substantially as described hereinbefore reference to and as shown in Figs. 1 and 5 of the accompanying drawings.

Printed in the United Kingdom for
Her Majesty's Stationery Office, Dd 8818935 1985
Published at The Patent Office, 25 Southampton Buildings
London, WC2A 1AY, from which copies may be obtained

APPENDIX 6: PUBLISHED PAPERS:

Reference to these published works in the text will be denoted by 'A' for exampl [A1]

1) C.H Oxley, A.M.Howard and J.J.Purcell 'Design and Performance of I-Band (8-10GHz) TRAPATT Diodes and Amplifiers' IEEE Trans MTT-27, nos.5, May 1979

2) 'C.H Oxley, T.J.Brazil, J.J.Purcell and R.Genner 'The design and performanc of J-band ferrite microstrip circulators' Proc.Inst.Elec Eng, vol 125, nos 8, pp 724- 727, Aug 1978.

3) C.H Oxley, A.M Howard and J.J Purcell 'X-band TRAPATT amplifiers Electron Letters, vol. 14, pp 416-418, 1977.

4) 'C.H Oxley, A.M Howard, S.M.R Gordon, and J.J Purcell 'High efficiency X band TRAPATT amplifiers and oscillators' Proc. 6th EMC, Rome, pp 311 315, 1976. Author presented the paper.

5) 'C.H Oxley, A.M.Howard and J.J.Purcell 'Design and performance c TRAPATT devices, oscillators and amplifiers' IEE SSED, vol.1, nos. 1, p 24-30, 1976. (The paper was an invited paper for the first edition of th SSED).

6) C.H Oxley 'Rugged Coaxial Microwave Cavity' Submission of invention 16/12/76.

Non first authored papers containing further research work carried out by the author:

7) M.W.Geen, T.J.Brazil and C.H.Oxley 'Locked oscillator power-combining through a Wilkinson Coupler' IEE Proc H, Vol 129, April 1982, pp 77-82.

A1

Design and Performance of *I*-Band (8–10-GHz) TRAPATT Diodes and Amplifiers

CHRISTOPHER H. OXLEY, ANTHONY M. HOWARD, AND JEFFREY J. PURCELL

Abstract—The design and fabrication of *I*-band silicon TRAPATT diodes are described, and the results of both oscillator and amplifier measurements are presented. The paper includes details of the design and characterization of a cascaded three-stage TRAPATT amplifier.

I. Introduction

THE HIGH-CONVERSION efficiency of the TRAPATT oscillator or amplifier makes it a contender for the solid-state replacement of TWT's at frequencies as high as 10 GHz. As oscillators, peak powers of 15 W have been demonstrated in *I* band with conversion efficiencies of up to 36 percent and as amplifiers, added-power efficiencies of 25 percent have been obtained. Duty factors as high as 12.5 percent have been realized with mean output powers in excess of 1 W.

This contribution describes circuit and diode design details and the characteristics of a three-stage TRAPATT amplifier operating at 9.6 GHz. The amplifier operates in a class-C mode, dissipating power solely during the pulse period, thereby maintaining peak efficiency from high duty factors to single-shot operation.

II. Device Design and Fabrication

Practical realization of *I*-band TRAPATT diodes requires careful consideration of many aspects of device production. The inpurity doping profile of the semiconductor material from which diodes are to be fabricated must be accurately controlled. Diode design and the method of fabrication must be directed towards producing a structure which provides efficient removal of heat from the device, and the devices ideally should be bonded into a package, the electrical and thermal properties of which impose minimal constraints upon the performance of the diode/circuit combination.

A. Material Growth and Characterization

The impurity doping profile of a conventional p^+-n-n^+ TRAPATT diode consists of a narrow n-type active region with abrupt p^+-n and n-n^+ interfaces. Under avalanche breakdown of the p^+-n junction, this structure is heavily punchthrough, the punchthrough factor F being defined by

$$F = \sqrt{\left(\frac{V_B}{V_P}\right)}$$

where V_B is the breakdown voltage of a nonpunchthrough diode with the same doping level and V_P is the punchthrough voltage.

The value of F for a practical TRAPATT diode is typically as high as six. It has been found, in practice, that devices with abrupt p^+-n junctions are prone to burn out at low input power levels, whereas those fabricated from material with a graded p^+-n region are able to operate reliably at current densities commensurate with high efficiencies. The n-n^+ interface, however, is designed to be as abrupt as possible in order to reduce parasitic loss under large-signal modulation.

Low-resistivity arsenic-doped substrates minimize the device parasitic resistance and produce a low-resistance ohmic contact. The high solubility of arsenic in silicon which is achievable ($\approx 5 \times 10^{19}$ atoms/cm^3) enables resistivities as low as 0.0015 Ω·cm to be realized. However, as arsenic is highly volatile, measures must be taken to contain it during any exposure of the silicon to high temperatures. The n-layer is grown by vapor phase epitaxy by the pyrolysis of silane. This method combines a high degree of doping and thickness control with a relatively low temperature (1075°C), thus minimizing n-n^+ interface degradation during growth. Prior to growth, a coating of silicon dioxide is grown at high temperature in steam to completely cover the substrate. Phosphorus-doped silicon is epitaxially grown onto the substrate through a window etched in the oxide. The oxide prevents the escape of arsenic from the substrate surfaces which would contribute to the n-layer doping in an uncontrollable manner.

Characterization of the n-layer doping level is achieved using a J.A.C. automatic profiler [1] in conjunction with a mercury Schottky-barrier diode on the surface of the grown layer. As the width of the n-type active region of the TRAPATT structure is critical and represents only about one-seventh of the total n-layer grown, it is essential that both growth and assessment are performed accurately. A mere 3.5-percent error in the total n-layer width may constitute an error of approximately 25 percent

Manuscript received June 10, 1978; revised November 2, 1978. This work was supported by the Procurement Executive of the United Kingdom Ministry of Defence, and partly sponsored by DCVD. It was published with permission of the Directors of Plessey Company, Ltd., Caswell, Towcester, Northants, England.

The authors are with the Allen Clark Research Center, Plessey Research (Caswell) Ltd., Caswell, Towcester, Northants, England.

0018-9480/79/0500-0463$00.75 ©1979 IEEE

in the relatively narrow active region width. The procedure for thickness assessment used is the jet etch and strain method [2] which delineates the n-n^+ interface, followed by an optical interference fringe method [3]. Measurement resolution of better than 500 Å representing approximately 1.5 percent of the total layer width is achieved.

The graded p^+-n junction is produced by depositing into the as-grown n-layer a shallow source of acceptor impurity atoms followed by a drive-in period at high temperature. The deposition has been effected both by thermal diffusion from oxidized boron nitride and by implantation of boron ions. The latter method is favored owing to the greater degree of control and reproducibility it affords. Early drive-in experiments using a pure inert gas environment were abandoned in favor of a 5-percent oxygen 95-percent inert gas (such as argon or nitrogen), as this gas mixture enhances the rate of diffusion of the boron atoms, leading to a reduction in the n-n^+ interface degradation. The drive-in, which lasts for approximately three hours and is performed at 1100°C, depletes the concentration of boron at the surface. This is replenished by a secondary low-temperature (860°C) diffusion of boron from an oxidized boron nitride source, resulting in low-resistance ohmic contacts without further effect on the rest of the impurity profile.

A sensitive check on the accuracy of the n-region width is the breakdown voltage of test diodes made from that material. For example, it has been empirically determined that optimum operation in the frequency range 8.5–9.5 GHz is achieved with devices with breakdown voltages between 28 and 34 V. Small adjustments to the drive-in time are sufficient to tailor the active region to the appropriate width. For operation in the frequency range 8–10 GHz, the complete material specification is as follows. A phosphorus-doped epitaxial layer, impurity concentration 7×10^{15} atoms/cm^3, thickness 3.6 μm, is grown onto an arsenic-doped substrate, impurity concentration 5×10^{19} atoms/cm^3. A dose of 5×10^{14} boron atoms/cm^2 is then implanted at 40 keV, to produce a peak concentration of 4×10^{19} atoms/cm^3. This is driven in for about three hours at 1100°C to produce an active region width of approximately 0.4 μm. The drive-in period also serves to anneal the implanted boron.

Finally, an 860°C, 30-min boron diffusion is effected to produce a 0.15 -μm p^+ contact layer. Fig. 1 illustrates the predicted final impurity doping profile.

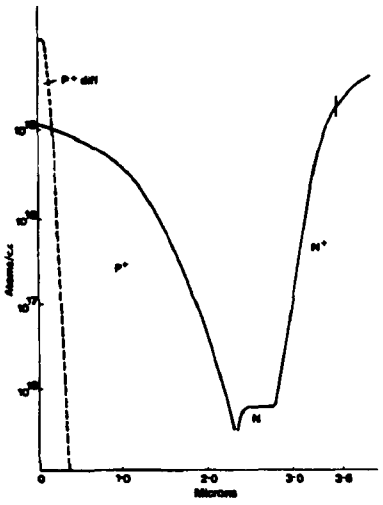


Fig. 1. *X*-band TRAPATT doping profile.

B. Device Thermal Design Considerations

Although the TRAPATT device has a relatively high efficiency, a substantial amount of dc power is dissipated as heat in the high field region. To maximize the dc power handling capability of the device and, hence, RF output, the junction must be provided with an efficient means of removing heat. TRAPATT's are generally operated in a pulse mode, thus both the mean and transient thermal response will determine the rate of change of temperature within the pulse, and also the maximum junction temperature at the end of each pulse, both of which limit the device RF performance and reliability. To minimize mean heating, integral-heat-sink (IHS) fabrication has been adopted. A high thermal conductivity metal is plated onto the device p^+ contact to provide a heat-sink as close as possible to the region of heat generation. The thermal impedance of the structure is reduced further by lapping the n^+ substrate to a minimum thickness, and then providing the n^+ contact with a second plated heat-sink [4] into which heat flows during the "on" time of the device. Heat flows in both directions from the junction during a pulse, providing the reservoir is close to the source of heat and with sufficient thermal capacity to act as a heat-sink. Heat flows from the reservoir through the device into the integral-heat-sink during the period between pulses. Choice of materials and dimensions for the two heat-sinks is determined by the pulse length, duty factor, and available fabrication technology.

C. Device Fabrication

The IHS fabrication procedure utilized in the production of TRAPATT diodes has been adopted from processes used in the production of high-frequency avalanche devices [5]. In order to minimize the thickness of silicon between the active region and the substrate contact (and, hence, minimize transient thermal impedance), an accurate substrate thinning process is adopted. The first stage in the fabrication process is to etch small diameter (approximately 50 -μm) holes into the p^+ side of

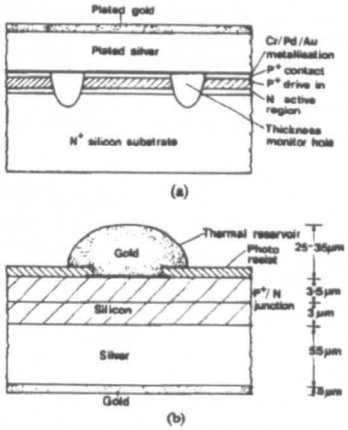


Fig. 2. (a) IHS TRAPATT fabrication process. (b) Final structure with thermal reservoir.

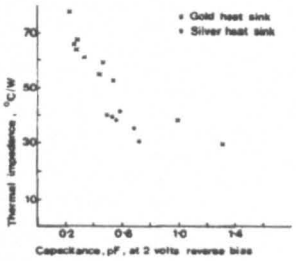


Fig. 3. A comparison between the CW thermal impedance of gold and silver heat sinks.

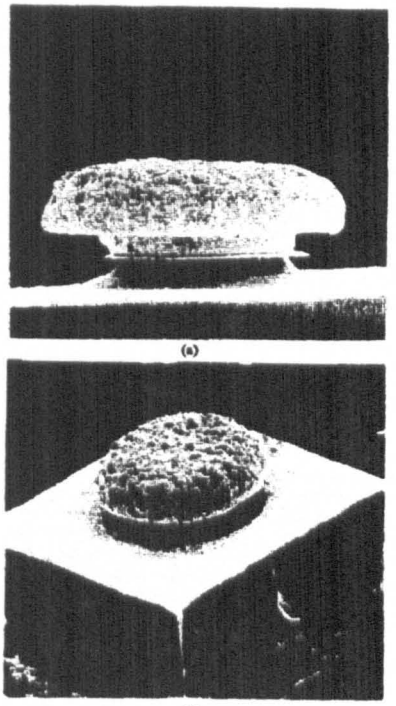


Fig. 4. (a) Completed TRAPATT diode. (b) Device with integral silver/gold heat sink.

the wafer to a depth equal to the required final silicon thickness. A metal contact is made to this face by the sequential vapor deposition of chromium, palladium, and silver. Onto the silver layer is then deposited approximately 55 μm of electroplated silver followed by 5 μm of electroplated gold, Fig. 2(a). A reduction in CW thermal impedance of approximately 20 percent has been achieved with this heat sink compared with that of an all-gold system used in earlier work [3], Fig. 3.

The silicon substrate is thinned by lapping and polishing with successively finer grits until the thickness monitor holes appear. The total silicon thickness at this stage is approximately 7–8 μm. Contact is then made to the n^+ substrate by vapor deposition of chromium, palladium, and gold. Circular contact areas are defined on this metal contact and gold heat reservoirs plated onto the areas through holes in a thick (3–5-μm) photoresist layer. Mesa devices are then defined by etching the silicon through to the p^+ contact metallization. Finally, devices are separated by cutting through the metal heat-sink. Fig. 4(a) and (b) illustrate the completed device.

D. Device Dimensional Design

The reverse-bias junction capacitances at breakdown of the TRAPATT diodes found to operate as oscillators or amplifiers in *I* band, lie in the range 0.25–1.20 pF, corresponding to junction areas from 0.3 to 0.8×10^{-4} cm^2. Minimum dimensions of the device integral-heat-sink are determined by the particular device junction area. If, for example, a device of junction area approximately 0.4×10^{-4} cm^2 is used, it has been found that a plated heat-sink 200-μm square comprising approximately 55-μm silver, 5-μm gold provides an adequately low steady-state thermal impedance when bonded into a suitable microwave package. Particular care must be taken in the choice of silver-plating solution and method of plating [6]. In order for the back-contact heat reservoir to be effective, it must have a large enough thermal mass for its temperature not to change appreciably during a pulse and it must be close

enough to the heat source to have effect during the pulse. From Fig. 2(b) it can be seen that the thermal paths to both integral-heat-sink and the thermal reservoir include approximately 3 μm of silicon with a thermal time constant of about 500 ns, consequently both plated regions are potentially effective heat-sinks for pulses in excess of half a microsecond duration. Plated reservoirs thicker than the 35 μm indicated in Fig. 3(b) do not significantly reduce the transient thermal impedance for 5-μs pulsewidths.

E. Device Packaging

Completed devices are ultrasonically bonded into AV162[1] microwave packages, the 5-μm gold-plated layer on the silver heat-sink being instrumental in obtaining good thermal intimacy between the device and package. A gold wire is then thermocompression-bonded to connect the device to the package rim.

III. Circuit Description

Stable fundamental frequency *X*-band TRAPATT reflection amplification has been obtained in both coaxial and microstrip circuits [3], [6], [8].

The TRAPATT amplifier circuit first investigated used a 50-Ω 3.5-mm diameter coaxial airline which supported a pure TEM mode to approximately 40 GHz [3]. A low-pass filter matching network was placed at less than the fundamental wavelength from the diode plane [9]. The circuit was very similar in configuration to that used in the time-domain-triggering (TDT) TRAPATT oscillator circuits described in the literature [10]. The appropriate matching network was realized by adjustment of three 20-Ω anodized aluminium slugs.

The diodes, as stated, were bonded in AV162 packages with high cutoff frequencies [11]. These circuits operated well giving gains of 7 dB with input signal levels of 1.2 W, and 3 dB with input signal levels of 5 W. Power-added efficiencies as high as 25 percent and bandwidths of 500 MHz were demonstrated [3]. However, this circuit tended to support spurious signals at frequencies corresponding to oscillator operation in the TDT mode. It was subsequently found that placing the filter network close to the diode package [12] eliminated these spurious signals.

This circuit arrangement also minimized the cavity slope reactance $dX/d\omega$, a necessary requirement for obtaining wide bandwidths, and enabled the efficient operation of larger area TRAPATT diodes. Provided the amplified signal was free from noise and pulse breakup, measurements over the frequency range of 2–18 GHz demonstrated that any spurious signals were 30–40 dB below the amplified signal.

The amplifier circuit contained a smaller number of matching sections than the conventional TRAPATT oscillator circuits [3]. The impedances and positions of the matching sections were empirically derived. The circuit consisted of a 50-Ω 3.5-mm diameter coaxial line, with the packaged diode mounted at the end of the line. A single low impedance 20-Ω section was placed close to the diode package, followed by a second, usually shorter, 20-Ω section. A pair of (TEFLON) inner supports were placed between the filter section and the bias network; these had a considerable influence upon bandwidth and the minimum signal level required to trigger the amplifier circuit. Variations in the circuit and package-bonding configurations were found necessary, depending upon the size of the diode to be matched. For example, a small area, 0.3×10^{-2}, diode of breakdown capacitance 0.25–0.35 pF required a high-inductance bonding configuration, a single 0.0012-cm diameter gold wire between the chip and the package, and a small PTFE slug 1.0 mm in length between the packaged diode and the first low impedance section of the matching network. Whereas larger area 0.8×10^{-4}-cm^2 devices of breakdown capacitance 0.6–1.3 pF required the first impedance matching section to be closer to the diode package and a lower inductance gold wire of diameter 0.0025 cm bonded between package and chip.

The operation of the amplifier using the circuit configuration described is not fully understood, as it precludes the classical TDT mechanism which is encountered in the TRAPATT oscillator. Mackintosh [13], [14] has described a simple theoretical circuit model for a TRAPATT oscillator which was not dependent upon the classical TDT mechanism. The model may go some way to explaining the operation of the TRAPATT amplifier, and is consistent with the wide negative resistance bandwidths observed. *I*-band TRAPATT amplifiers operating with pulses of the order of 0.5 μs and duty factors of 1 percent have shown 3-dB gain bandwidths of greater than 11 percent with maximum gain of 5 dB. The usable bandwidth was smaller, as there were regions of noisy operation where the device was no longer optimally matched.

A. Biasing Techniques

The TRAPATT amplifiers were operated in class C [15] by biasing the diode below its breakdown voltage. In this state, the diode was in effect switched-off, and negligible current flowed through it. When an RF signal of sufficient amplitude was applied, the TRAPATT mode was triggered, the voltage dropped below the bias voltage, a large current flowed through the diode, and RF amplification occurred. In the absence of the RF signal, the diode returned to its off-state, with negligible current flow. Biasing was applied by a dc voltage just below the breakdown voltage of the diode. A resistance–capacitance network in the biasline absorbed the diode voltage dropback, as the diode switched into the TRAPATT mode and suppressed ringing in the bias circuit. Small area diodes, 0.3×10^{-4}cm^2, with breakdown capacitances of the order of 0.3 pF, and operating at a current level of 300–400 mA, required a bias load resistance of approximately 12 Ω. Larger area diodes 0.8×10^{-4}cm^2 with breakdown capacitances of 1 pF, operating at a current level of greater than 1 A, required a bias load resistance of 2–4 Ω. In practice it

[1] Lectronics, Inc.

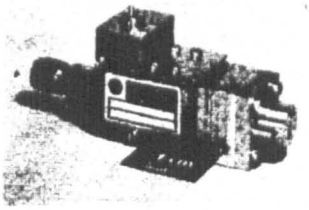


Fig. 5. Rugged TRAPATT amplifier cavity.

was found to be important to operate at the correct dc load-line point, otherwise noisy and unstable operation was obtained, often accompanied by limited bandwidth and poor RF rise-time. Voltage spikes on the average voltage switching waveform could be suppressed by including ferrite beads in the bias circuit line, these helped to reduce spike-induced burnout, with little degradation in RF rise-time, this being typically 40–60 ns for a single-stage TRAPATT amplifier.

B. Ruggedized Coaxial Circuit

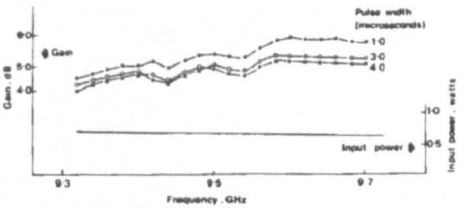
To fulfill systems requirements of tolerance to vibration and shock, a novel, rugged TRAPATT cavity with internal biasing (Fig. 5) was developed. The cavity consisted of a number of metal plates of various thicknesses which were mounted together to reproduce the characteristics of the slug-tuned cavity. Shims were used to adjust the relative positions of the matching sections, so providing fine tuning. The plates were located by dowels and could be clamped firmly together to produce a rugged TRAPATT amplifier circuit. The cavity could withstand a vibration of 23-g rms over a spectrum of 10–2000 Hz, without a measurable degradation of the microwave performance.

IV. Microwave Performance

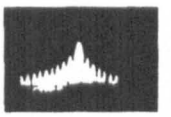
The TRAPATT amplifiers have been operated with power-added efficiencies as high as 25 percent in *I* band [3], whereas *I*-band TRAPATT oscillators have given efficiencies in excess of 35 percent [16], [17].

The TRAPATT amplifier requires a minimum input signal level before amplification is initiated. The threshold input signal level depends upon the area of the device, small area devices requiring levels of the order of 0.5 W, and larger area devices 1–3 W. With increasing signal drive level, the gain characteristic is linear at 3–7 dB, before going into saturation and finally compression. The TRAPATT device is essentially suited to large-signal low-gain applications.

To obtain the most effective power budget in cascaded amplifier design, it is necessary to use small area devices in the initial stages and larger area diodes in the output stages. Small area diodes, corresponding to breakdown capacitance 0.25–0.35 pF, allow the operation of efficient TRAPATT reflection amplifiers with an input signal drive level of 500–700 mW. At pulsewidths of 1 μs and duty factors of 1 percent, gains greater than 6 dB with 1-dB



(a)



(b)

Fig. 6. (a) TRAPATT amplifier with varying input pulsewidth. (b) Amplified 4-μs pulse spectrum.

bandwidths in excess of 400 MHz at a center frequency of approximately 9.4 GHz have been obtained at maximum power-added efficiency of approximately 16 percent. Gains of 8 dB with power-added efficiencies in excess of 18 percent have been obtained over narrower 1-dB bandwidths, 170 MHz, again centered at approximately 9.4 GHz. For many systems applications it is necessary that the device operates over long pulsewidths. Fig. 6(a) shows the operation of a TRAPATT amplifier with an input of approximately 600 mW and pulsewidths between 1 and 4 μs making use of the improved thermal structure as discribed earlier. Fig. 6(b) shows the frequency spectrum for an amplified 4-μs pulsewidth. Devices have been operated with pulselengths of greater than 8 μs with gains of 4 dB over 1-dB bandwidths of 400 MHz centered at 9.3 GHz. For long pulsewidth operation, it was experimentally determined that devices with low leakage currents of the order of 100 nA were less prone to tuning induced burnout.

The S_{11} parameters at the diode package plane for both amplifier and oscillator circuits have been measured between 8 and 12 GHz using an HP network analyzer. The measurements indicated that the amplifier circuit impedance at the fundamental frequency had a real component of 10–20 Ω, compared with 5–8 Ω for the oscillator. The impedances suggest that larger area diodes should be more readily matched as amplifiers, and this has been experimentally verified. Fig. 7 shows that the added-power efficiency of an amplifier decreases with increasing device breakdown capacitance, whereas the oscillator shows a linear decrease in efficiency with device breakdown capacitance.

For large input signal levels of 3.6 W over 0.5-μs pulsewidth with a 1-percent duty factor, Fig. 8 shows the bandwidths obtained for a range of diodes with breakdown capacitances between 0.94 and 1.2 pF. The added power efficiency was as high as 20 percent with gains of about 3 dB.

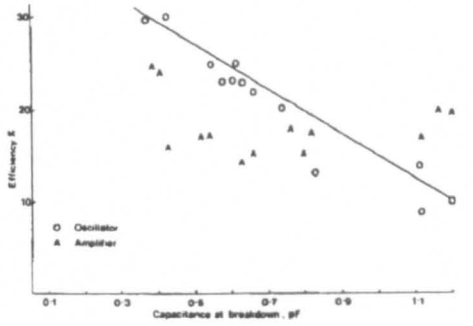


Fig. 7. Efficiency of amplifier and oscillator versus diode breakdown capacitance.

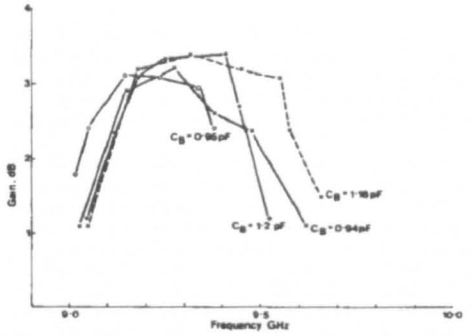


Fig. 8. Large input signal amplification.

A. *Cascaded* TRAPATT *Amplifiers*

To increase the gain and peak power of the amplifier, TRAPATT class-C reflection amplifiers have been cascaded. Fig. 9(a) shows the gain-frequency response of a two-stage cascaded TRAPATT amplifier constructed with SMA coaxial circulators. The first stage contained a diode of breakdown capacitance of approximately 0.3 pF, and the second stage used a larger area device with a breakdown capacitance of 0.6 pF. With an input signal of 550–700 mW, a pulsewidth of 1 μs, and a 1-percent duty factor, an overall gain of 9.5 dB was realized. Fig. 9(b) shows the amplified 1-μs pulse spectrum. Isolation between the stages was found to be necessary to reduce noisy operation. The amplifier operated in the class-C mode from dc supply rails and used a capacitance–resistance load line as previously described. The feasibility of this unit being driven by an FET driver stage was demonstrated. The overall gain of the complete unit including the FET driver stage was 26 dB, with a maximum output power of 4.6 W and a 1-dB bandwidth in excess of 200 MHz at a center frequency of 9.4 GHz.

By utilizing integrated microstrip circulators and isocirculators, and coupling miniature TRAPATT cavities

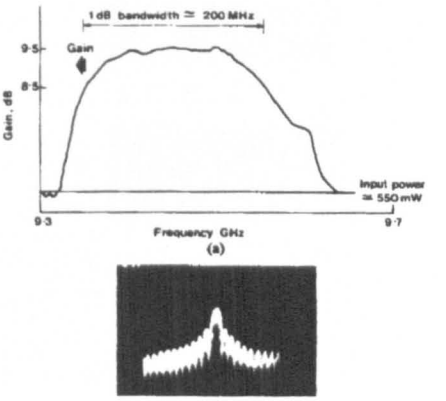


Fig. 9. (a) Cascaded TRAPATT amplifier gain response. (b) Amplified 1-μs pulse spectrum.

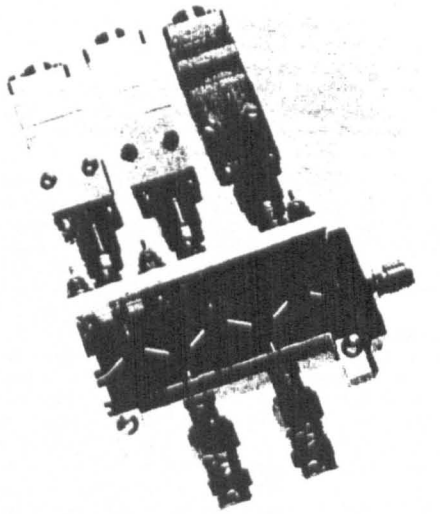


Fig. 10. Three-stage TRAPATT amplifier assembled using microstrip circulators and isocirculators.

via OSM launchers to the microstrip circuit, a complete three-stage TRAPATT amplifier was assembled and is shown in Fig. 10. Both thick and thin film techniques were used to fabricate circulators, isocirculators [19], bias filters, and dc blocks on a single 5.08×2.54-cm ferrite substrate. The microstrip circuit was assembled in a box lined with lossy material so as to reduce box-made resonances. The TRAPATT cavities were a miniaturized form of the 3.5-mm diameter 50-Ω coaxial ruggedized circuit already described. The unit gave a gain of 9–10 dB with

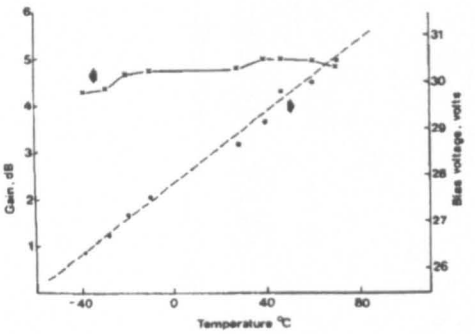


Fig. 11. Operation of TRAPATT amplifier over a temperature range.

an output peak power in excess of 10 W, with an overall added power efficiency of approximately 7 percent for pulsewidths between 0.5 and 1.0 μs at a center frequency of 9.7 GHz. The cascaded TRAPATT amplifiers showed a degradation in RF rise-times and an increase in switch-on delay.

Cascaded TRAPATT pulsed, class-C amplifiers have been demonstrated, but difficulties were experienced in obtaining an added power from each successive amplifier stage. The problem was thought to be a result of having poor harmonic isolation between stages. The isolation between stages was measured as greater than 50 dB at the fundamental frequency of 9.7 GHz, but would be relatively poor at the harmonics. Consequently, each successive TRAPATT stage provided a harmonic mismatch to the preceeding TRAPATT stage, causing noisy and low gain operation. However, by adjusting the line lengths between stages, some degree of tuning could be effected enabling successful operation of multiple cascaded reflection TRAPATT amplifiers.

As with the majority of solid-state devices, the TRAPATT requires subsidiary electronic circuitry to provide protection, temperature compensation, and correction of intrapulse phase shift with increasing pulsewidth, in order to maximize the versatility of the amplifier. These circuit techniques are described below.

B. Temperature Performance

A large-signal amplifier giving a maximum gain of 5 dB at a center frequency of 9.5 GHz has been operated over a temperature range of −40–70°C, with a maximum variation in gain of 0.75 dB. This was obtained by linearly increasing the bias voltage by approximately 12 percent with increasing temperature (Fig. 11).

C. Intrapulse Phase Variation

The TRAPATT diode junction temperature rises rapidly with increased pulse lengths causing transient impedance changes with consequent droop in gain across the pulsewidth of the amplified signal and a reduction in the overall efficiency of the amplifier. It was experimentally

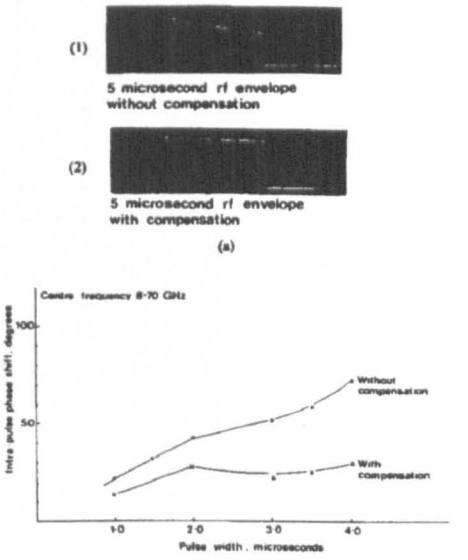


Fig. 12. (a) A comparison between an amplified 5-μs RF envelope without and with electronic compensation. (b) Intrapulse phase of a single stage TRAPATT amplifier.

observed that there was approximately a linear increase in intrapulse phase shift as the amplified pulse was lengthened. For a single-stage TRAPATT amplifier, an amplified 4-μs pulsewidth resulted in a total intrapulse phase shift of 100°. Both gain reduction and intrapulse phase shift are undesirable in pulse compression radars and many other systems applications.

A simple method of minimizing both gain droop and intrapulse phase shift with increasing pulsewidth was developed for the class-C TRAPATT amplifier. This consisted of an electronic compensation circuit which derived its trigger from the voltage drop-back which resulted across the TRAPATT diode when an RF input signal was applied to the amplifier. The trigger circuit switched off with the voltage recovery, on removal of the RF input signal. The trigger signal was, therefore, approximately the length of any input signal applied to the amplifier and was used to initiate a variable exponential current source. This was superimposed upon the current being drawn from the constant voltage supply, thus shaping the current waveform to the TRAPATT device. Significant improvements in both gain and intrapulse phase were observed. Fig. 12(a) shows a comparison between an amplified 5-μs RF envelope from both an uncompensated and a compensated TRAPATT amplifier. An improvement in gain of 12–20 percent for a single stage TRAPATT amplifier could be realized, and it was also noted that there was an improvement in bandwidth for long pulsewidth operation. Without compensation, a 4-μs amplified pulse showed a

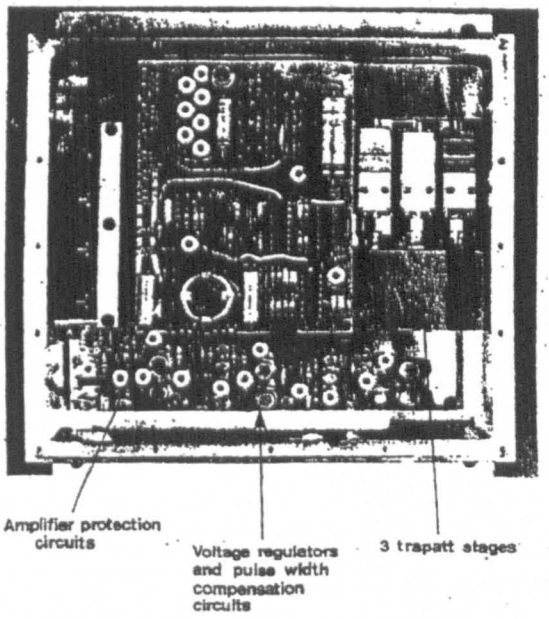


Fig. 13. Three-stage class-C TRAPATT amplifier with protection and pulse compensation circuitry.

3-dB bandwidth of approximately 270 MHz, whereas with compensation the identical amplifier showed a 3-dB bandwidth of greater than 400 MHz. Fig. 12(b) demonstrates significant improvements in intrapulse phase across the pulse; for a 4-μs pulsewidth the phase shift was greater than 70°, whereas with compensation this was reduced to less than 30°. Obviously, further improvements could be obtained if the relationship between temperature and pulsewidth were determined and exactly compensated for, rather than the first-order approximation adopted.

Fig. 13 shows a completed 10-W TRAPATT amplifier. It consisted of three TRAPATT reflection amplifier stages linked together by microstrip circulators and isocirculators as described. The complete unit was supplied from a single 36-V rail, and the voltage to each TRAPATT stage was controlled by voltage regulators, allowing the appropriate breakdown voltage to be set for each diode. The amplifier stages were electronically compensated, to regulate both gain and intrapulse phase variations with pulsewidth. To protect the TRAPATT diodes and electronic circuitry, a current limit and an excess voltage switch were included. To afford protection against a quasi-CW input signal, an input pulsewidth limiting circuit was added. This circuit compared the length of pulse derived from the voltage drop-back across the TRAPATT diode with a predetermined value, which could be set in the range from 1 to 10 μs. If this value were exceeded, then the supply rail to the TRAPATT amplifiers was electronically switched off in approximately 500 ns.

D. Efficiency of Overall Unit

Despite the high intrinsic efficiency of each TRAPATT device, the efficiency of the basic three-stage cascaded amplifier was reduced to approximately 7 percent when the losses and compromises in the microwave circuit were included. Addition of the electronic circuitry with its inherent loss further reduced the efficiency significantly. This is typical of the degradation that occurs from a laboratory state-of-the-art unit to a system prototye.

V. Conclusions

The development of silicon TRAPATT diodes and improved circuit techniques has resulted in the demonstration of efficient *I*-band TRAPATT pulsed amplifiers. The successful operation of the TRAPATT device with power FET driver stages, microstrip technology, and electronic circuitry for the correction of intrapulse phase deviation, demonstrated that the TRAPATT, like other solid-state devices, can be integrated into relatively complex subsystems.

Cascading reflection TRAPATT amplifiers has been shown to be feasible, but difficulties were experienced in obtaining the expected added powers and gains, which

155

consequently led to an overall efficiency of approximately 7 percent for a three-stage amplifier.

The *J*-band TRAPATT oscillator results of 15 W with 36-percent conversion efficiency are comparable with the state-of-the-art short-pulse (500-ns) operation of modified-Read-profile GaAs IMPATT's (16.8 W at 9.3 GHz at 32 percent). However, the inherently thinner active region width (0.3 μm versus approximately 2.5 μm) enables the TRAPATT to be operated over greater pulsewidths. The diodes described in this paper suffered a thermal penalty of about 3 μm of p^+ contact material. It is anticipated however, that attention to reduction of the contact region width would enable operation to be extended from the present limit of about 7 μs to periods in excess of 20 μs with a corresponding increase in mean operating levels. The complexity of circuit matching requirements probably limits fundamental TRAPATT operation to about 12 GHz, though the potential of harmonic extraction remains to be determined.

As an amplifier, the TRAPATT's unique voltage "cutback" characteristic enables operation in a class-C mode to be readily achieved. Alternative high-efficiency amplifiers may exhibit comparable performance over the operating pulse; however, their mean efficiency would be small in low duty-cycle operation. TRAPATT operation in class C permits overall efficiencies in excess of 20 percent to be realized for a range of duty factors and pulsewidths making the device suitable for ECM applications.

Acknowledgment

The authors would like to thank P. K. Shaw for material growth and S. M. R. Gordon for the fabrication of the TRAPATT diodes, F. F. Kemp for the design and many useful discussions on the electronic circuits for the TRAPATT amplifier, and J. K. Hemming for the electronic circuit layouts and construction. Thanks should also be given to A. L. Edridge, P. R. Wickens, and M. R. Weatherhead for their previous contributions.

The authors would especially like to thank I. W. Mackintosh and R. J. Royds of the R.S.R.E. Malvern, for many useful and encouraging discussions throughout the development of these devices and amplifiers.

References

[1] P. J. Baxandall, D. J. Colliver, and A. F. Frag, "An instrument for the rapid determination of semiconductor impurity profiles", *J. Phys. E.*, vol. 4, pp. 213–221, 1971.

[2] R. W. Bicknell, "A simple rotating jet-thinning apparatus for producing taper sections and electron microscope specimens from silicon and compounds semiconductors," *J. Phys. E.*, vol. 6, pp. 1991–1997, 1973.

[3] C. H. Oxley, A. M. Howard, and J. J. Purcell, "Design and performance of TRAPATT devices, oscillators and amplifiers," *IEE SSED*, vol. 1, no. 1, pp. 24–30, 1976.

[4] W. R. Cartice, J. J. Risko, and P. T. Ho, "A study of second-harmonic-extraction TRAPATT amplifiers for *X*-band operation," *RCA Rev.*, vol. 36, pp. 274–295, 1975.

[5] A. M. Howard, D. Smith, and J. J. Purcell, "Epitaxially grown double-drift silicon IMPATT diodes at 60 to 90 GHz," *Electron. Lett.*, vol. 10, no. 21, pp. 443–444, 1974.

[6] K. Sheppard and J. P. G. Farr, Dept. Metallurgy, Univ. of Birmingham, United Kingdom, private communication.

[7] C. H. Oxley, A. M. Howard, and J. J. Purcell, "*X*-band TRAPATT amplifiers," *Electron. Lett.*, vol. 14, pp. 416–418, 1977.

[8] C. H. Oxley, A. M. Howard, S. M. R. Gordon, and J. J. Purcell, "High efficiency *X*-band TRAPATT amplifiers and oscillators," in *Proc. 6th EMC*, Rome, Italy, pp. 311–315, 1976.

[9] I. W. Mackintosh, "Circuit model for TRAPATT-oscillator cavities," *Proc. Inst. Elec. Eng.*, vol. 119, no. 11, pp. 1529–1537, Nov. 1972.

[10] W. J. Evans, "Circuits for high-efficiency avalanche diode oscillators," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-17, pp. 1060–1067, 1969.

[11] I. W. Mackintosh, R. J. Royds, and R. G. T. Morris, "A technique for the characterization of microwave diode packages and mounts," *IEEE Trans. Microwave Theory Tech.*, to be published.

[12] M. I. Grace, "Broadband high-efficiency-mode amplifiers at *S*-band," in *Proc. EMC*, Stockholm, Sweden, 1971.

[13] I. W. Mackintosh, "Charge generation in TRAPATT diodes," *Electron Lett.*, vol. 13, no. 8, pp. 231–233, 1977.

[14] ——, "An equivalent circuit model for TRAPATT diodes," in *Proc. 6th Cornell Conf.*, 1977.

[15] A. Rosen, J. E. Reynolds, S. L. Liu, and G. E. Theriault, "Wide-band class-C TRAPATT amplifiers," *RCA Rev.*, vol. 33, pp. 729–736, 1972.

[16] J. J. Purcell, M. R. Weatherhead, S. M. R. Gordon, C. H. Oxley, and P. R. Wickens, "High efficiency TRAPATT operation in *X*-band," *Electron. Lett.*, vol. 11, pp. 236–238, 1975.

[17] T. T. Fong and R. S. Ying, "Complementary *X*-band TRAPATT diodes," presented at the IEEE Int. Microwave Symp., Atlanta, GA, June 1974.

[18] C. H. Oxley, T. J. Brazil, J. J. Purcell, and R. Gosner, "The design and performance of *J*-band ferrite microstrip circulators," *Proc. Inst. Elec. Eng.*, vol. 125, no. 8, pp. 724–726, Aug. 1978.

Design and performance of J-band (12·4–18 GHz) ferrite microstrip circulators

C.H. Oxley, B.Sc., T. J. Brazil, B.Eng. (Elec.), Ph.D., M.I.E.E.E., J.J. Purcell, M.Sc., Ph.D., M.Inst.P., C.Eng., M.I.E.E., R. Genner, B.Sc.

Indexing terms: Circuit computer-aided design, Ferrite devices, Microwave integrated circuits, Strip lines

Abstract

A computer program CIRFER is described that facilitates the design of circulators on all-ferrite substrates. With the use of the design approach, J-band circulators have been fabricated using thin-film techniques on ferrite substrates of different $4\pi M_s$ values. Good agreement was obtained between theoretical and experimental resonant-disc diameters at the centre frequency of operation of the circulator. The circulators gave isolations of 20–40 dB in mid J-band, with a corresponding loss per pass of the order of 0·5 dB. The microwave performance is sufficiently encouraging to suggest that in certain applications an all-ferrite approach could be considered, which would simplify the circulator design. The computer program CIRFER has been filed with the IEE Computer Program Library.

1 Introduction

This paper reports measurements on J-band ferrite microstrip circuits, and describes a computer program developed for the design of circulators on ferrite substrates.

Ceramic substrates are conventionally used for microstrip circuits to frequencies as high as the Q-band (26·5–40 GHz).[1] Nonreciprocal components such as circulators and isolators utilise magnetically biased ferrites to effect the required r.f. field rotation. These components are fabricated by inserting a disc of ferrite of diameter slightly greater than that of the resonant element of the circulators into the ceramic substrate. The process of embedding the ferrite into the ceramic is mechanically complex and may be financially prohibitive in the case of circuits containing a number of circulators fabricated on the same substrate.[2] In applications subject to extreme environmental conditions, ferrite inserts may have to be deposited by arc plasma spraying of ferrite powder,[3] further increasing cost and fabrication difficulties.

The use of all-ferrite substrates has previously been restricted to frequencies below the X band by excessive r.f. losses at higher frequencies. However, recent improvements in material quality and surface finish have now enabled their use to be extended to frequencies as high as 18 GHz. Fig. 1 shows the total r.f. loss measured between 14 and 16 GHz on a 50Ω line fabricated on a 2·54 cm (1 in) 0·635 mm (0·025 in) thick Trans Tech TT1-3000 ferrite substrate with a surface finish of less than $2{\cdot}54 \times 10^{-6}$ cm (10^{-6} in) c.l.a. The transmission loss includes the effect of two Cable-Wave SMA coaxial to microstrip launchers. The loss figures obtained on the ferrite substrates were comparable with those measured on a 2·54 cm (1 in) length of ceramic substrate with two microstrip to coaxial launchers.

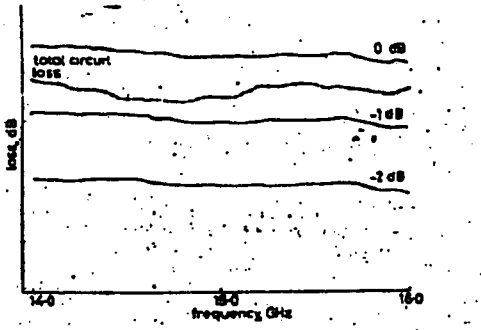


Fig. 1
Total r.f. loss of 50 Ω line on ferrite substrate

The use of a ferrite substrate substantially reduces the cost of circulators and isolators, simplifies the design, and minimises mechanical stresses under extreme environmental conditions.

2 Theoretical design of circulator

A computer program CIRFER has been developed, based on work by Genner*, for the design of circulators on ferrite substrates. The user specifies the substrate thickness h, the relative dielectric constant ϵ_r and saturation magnetisation $4\pi M_s$ of the ferrite substrate, the conductor metallisation thickness, and the centre frequency of operation. The program calculates the metallisation radius of the circulator, the length and width of the matching transformers and the 50 Ω linewidth at the centre frequency of circulation, and predicts the bandwidth over which the v.s.w.r. is less than a value supplied by the user.

In calculating the circulator metallisation radius, it is important to allow for the fringing magnetic fields around the resonant disc which lead to an effective radius (r_{eff}) which is in excess of the physical radius (r_0). The effective radius is calculated using the following expression, quoted by Wolff and Knoppik:[5]

$$r_{eff} = r_0\left(1 + \frac{2h}{\pi r_0}\left(\ln\left(\frac{\pi r_0}{2h}\right) + 1{\cdot}7726\right)\right)^{1/2} \qquad (1)$$

The calculations of impedances and linewidths are based on the recent paper of Wheeler,[4] and include the effects of the nonzero metallisation thickness on the impedance calculations.

Fig. 2 shows a theoretical plot of circulator metallisation radius against centre frequency of operation for two ferrites of different values of $4\pi M_s$. Circulators manufactured using the design procedure

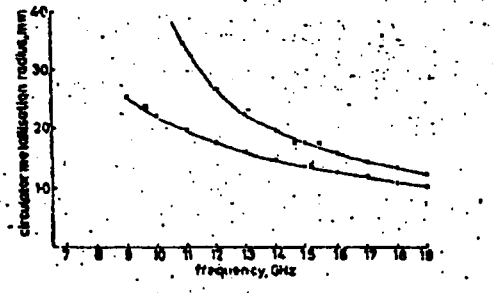


Fig. 2
Circulator metallisation radius as a function of frequency

•TT1-3000 ferrite, $4\pi M_s = 0{\cdot}3$ Wb/m²
▪G1001 ferrite, $4\pi M_s = 0{\cdot}12$ Wb/m²
x experimental points

*Unpublished work

Paper CP158E, first received 6th February and in revised form 26th April 1978. The program and accompanying documentation are held in the IEE Computer Program Library, IEE, Savoy Place, London WC2, England. Copies are available on application and on payment of a charge of £7·50

Mr. Oxley, Dr. Brazil and Dr. Purcell are with Plessey Research (Caswell) Ltd., Allen Clark Research Centre, Caswell, Towcester, Northants, England, and Mr. Genner is with RSRE, St. Andrews Road, Great Malvern, Worcs., England

The magnetic permeability of ferrite varies with frequency the variation being most pronounced at the magnetic-resonance frequency of the ferrite is approached. The results from Wheeler's paper must be modified using an effective value for the relative permeability (μ_{eff}). The intrinsic relative permeability of unmagnetised ferrite as a function of frequency is described by the expression:[4]

$$\mu(f) = \frac{1}{3}\left[1 + 2\cdot\left(1 - \left(\frac{\gamma 4\pi M_s}{f}\right)^2\right)^{-1/2}\right] \qquad (2)$$

where

$$\gamma = 0{\cdot}28\,\mathrm{GHz m^3/wb}$$

This value is transformed to an effective permeability for the microstrip structure using the formulation derived by Pucel and Masse,[6] and used to determine the impedances and corresponding microstrip linewidths.

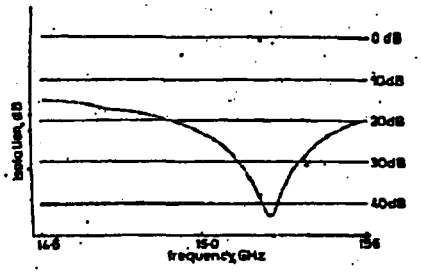


Fig. 3
Circulator isolation using ferrite with a $4\pi M_s$ value of 0·12 Wb/m²

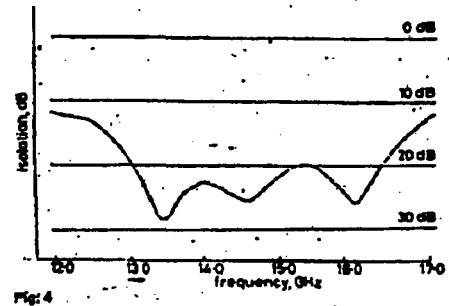


Fig. 4
Circulator isolator using ferrite with a $4\pi M_s$ value of 0·3 Wb/m²

3 Experimental results

With the use of the design procedure described above, a circulator was designed to operate at a centre frequency of 15 GHz, on Trans-Tech G1001 material, which has a saturation magnetic field of 0·12 Wb/m². The predicted bandwidth for an input v.s.w.r. of less than 1·2 was 850 MHz, and the measured bandwidth was 900 MHz. Fig. 3 illustrates the experimental operation of the circulator, showing a maximum isolation of greater than 40 dB at 15·2 GHz, and an isolation bandwidth of 580 MHz. The total loss of the circulator, 2·54 cm (1 in) of 50 Ω line and coaxial to microstrip launchers was of the order of 1 dB, while the loss of 2·54 cm (1 in) of 50 Ω line was approximately 0·6 dB, thus giving a loss per pass of 0·4 to 0·6 dB.

A similar design has been fabricated on Trans-Tech TT1-3000 material, which has a saturation magnetisation field of 0·3 Wb/m². The higher saturation field allows wider bandwidths to be realised. Fig. 4 shows a 20 dB isolation bandwidth of 3·4 GHz at a centre frequency of 14·05 GHz.

The designed input v.s.w.r. bandwidth was 3·8 GHz at a centre frequency of 15·0 GHz. The circulators were magnetically biased using small samarium-cobalt permanent magnets,[7] and a cylinder of ferrite of the same diameter as the metallised disc was placed on the resonator to improve the homogeneity of the magnetic flux through the circulator.

Microstrip lines on ferrite substrates have shown r.f. losses in the J band that are comparable with those obtained on ceramic substrates. An all-ferrite approach simplifies circulator design, and if a large number of circulators and isolators are required on a single substrate, for example in multistage reflection amplifier,[2] then fabrication cost is reduced. The approach should also be applicable to circuits required to function under extreme environmental conditions, which would cause the epoxy resin bonding a ferrite puck into a ceramic substrate to be excessively stressed. The computer program CIRFER has been filed with the IEE Computer Programs Library.

5 Acknowledgments

This work has been carried out with the support of the Procurement Executive of the UK Ministry of Defence, and is published with the permission of the Directors of Plessey Research (Caswell) Ltd.

6 References

1 BRIGGINSHAW P.M., and RICHES E.F.: 'Development of m.i.c. circulators from 1 to 40 GHz', *IEEE Trans.*, 1975, Mag-11, pp. 1273–1275
2 GENNER R., RICHMOND W., and BRADDOCK P.W.: 'Thick-film 3-stage m.i.c. impatt-diode amplifier on ferrite', *Electron. Lett.*, 1977, 13, pp. 193–195
3 WOLFF I., and KNÖPPIK N.: 'Rectangular and circular microstrip disk capacitors and resonators', *IEEE Trans.*, 1974, MTT-22, pp. 857–864
4 WHEELER H.A.: 'Transmission-line Properties of a strip on a dielectric sheet on a plane', *IEEE Trans.* 1977, MTT-25, pp. 631–646
5 MASSE D. J., and PUCEL R.A.: 'Microstrip propagation on magnetic substrates – Part II: Experiments', *IEEE Trans.* 1972, MTT-20, pp. 309–313
6 PUCEL R. A., and MASSE D.J.: 'Microstrip propagation on magnetic substrates – Part I: Design theory', *IEEE Trans.* 1972, MTT-20, pp. 304–308
7 BRIGGINSHAW P.M., LANCASTER N.M., SWALLOW G.H., and OXLEY T.H.: 'Some recent advancements in hybrid m.i.c.s', 7th European Microwave Conference, Copenhagen, 1977, pp. 446–449

7 Program description

7.1 Problem description for program CIRFER

The purpose of the computer program CIRFER is to provide design information facilitating the manufacture of microstrip circulators on all-ferrite substrates, assuming an operating frequency in excess of the magnetic-resonance frequency of the ferrite. This resonance frequency (in GHz) is determined as 0·28 times the saturation magnetisation ($4\pi M_s$, in Wb/m²). If a centre frequency is specified equal to or less than this value, the program returns an error message, and fails to operate. With reference to the flowchart (Fig. 5), the next item calculated is the physical radius r_0 of the circulator disc. As described by Genner,[3] the condition for resonance in the disc is given by:

$$\frac{2\pi f_0}{c}\sqrt{\epsilon_{eff}\mu_{eff}}\,r_{eff} = 1{\cdot}84 \qquad (3)$$

where f_0 is the centre frequency, c the speed of light in free space, and ϵ_{eff} and μ_{eff} represent effective permittivity and permeability, respectively. A curve relating ϵ_{eff} to r_0 given by Genner has been represented by a second-degree polynomial for use in the program. The effective radius r_{eff} is also a function of r_0 as shown in eqn. 1. Thus eqn. 3 describes a nonlinear equation in r_0 which can be solved numerically.

For matching the circulator at the centre frequency, a value is required for the circulator conductance (the susceptance being zero at this frequency). It is shown by Genner that the conductance is inversely proportional to the microstrip linewidth W of the matching transformer sections. The width is also related to the conductance through the usual condition for a quarter-wave impedance match. Hence W is also defined by a nonlinear algebraic equation which may be solved numerically.

The effective permittivity and permeability of the unmagnetised ferrite are then calculated, and used to determine the length of the matching sections.

Finally, the program addresses the synthesis problem of obtaining the width of line required to provide a 50 Ω impedance in the connecting microstrip circuit. Although an explicit expression for width in terms of impedance is quoted by Wheeler,[4] the presence of a permeability term in the present case results in a width which is only known implicitly, and so must be determined as the root of another nonlinear algebraic equation.

(a) Program name: CIRFER
(b) Author: T. J. Brazil
(c) Language: Fortran IV
(d) Number of variables: 117 (estimated)
(e) Special word-length requirements: none. Single precision arithmetic used throughout (32 bits/real variable)
(f) Number of statements: 302
(g) Input data stream number: 5
(h) Output data stream number: 6

7.3 Performance guide

(a) Computer used: MODCOMP IV/25
(b) Core size required: about 20k bytes
(c) Input medium: paper tape, 8 hole, ASCII code
(d) Output medium: Line printer
(e) Work or data files needed: one input (data) file, one output file
(f) Time taken to run submitted problem: 1·35 s
(g) Limitations: aside from the constraint requiring an operating

the root-finding routine. Clearly, the range over which solutions is to be sought has to be specified. For the circulator disc radius and the transformer section width, the solution is assumed to lie in the range 0·1 mm to 1·0 cm. This range should cover most practical applications of the program; however, in the event of a change becoming necessary, the relevant statement numbers in the program are 47 and 48. The limits chosen for the calculation of bandwidth are half the centre frequency (or the magnetic-resonant frequency if this larger) to 1·5 times the centre frequency. The relevant statement numbers here are 88–92 inclusive.

It has been assumed in the program that the external line impedance required is 50 Ω. Should a different value be required, the value of Z0 given in statement 60 may be changed accordingly. This is related to the boundaries set for the ratio of external line-width to substrate height, in the last application of the root-finding routine (see statement 104). The actual range allowed is 0·1 to 20, which, from a study of a number of ferrite materials, has been found to correspond to an impedance range of approximately 10 to 100 Ω.

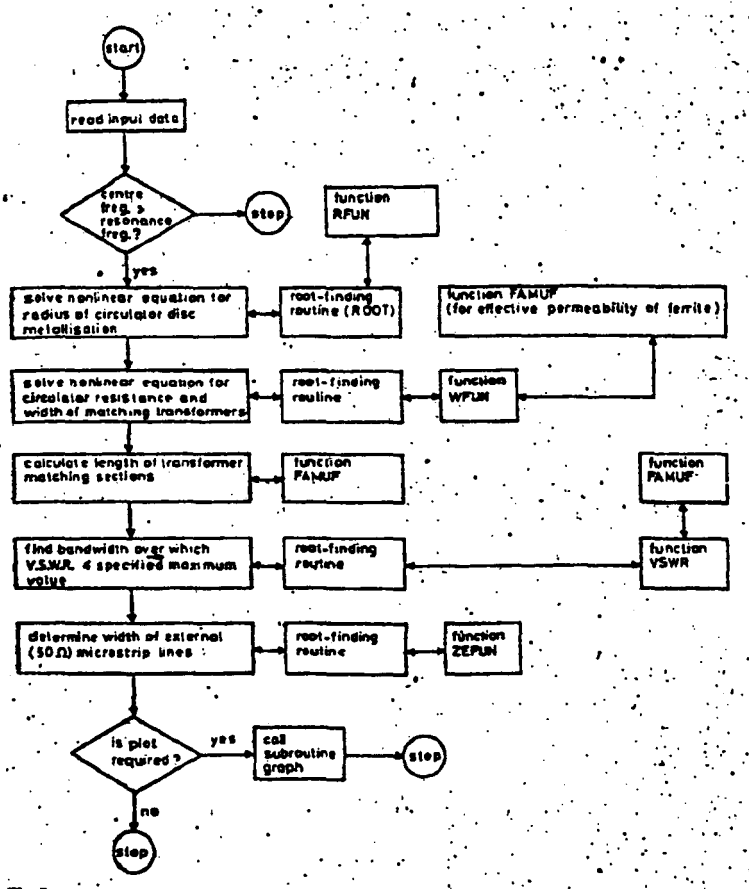


Fig. 5
Program flowchart

§ Private communication

which, in the context of a radar, means that it is reset at the beginning of each time window of interest and only pulses which fire the tunnel diode during the time window are counted as 'hits'. The tunnel-diode threshold is adjusted by a feedback loop so that, during these successive time windows at the repetition rate of the system, the false-alarm rate due to noise triggering the diode is perhaps 1/16. However, a signal is assumed to be present within the time window only if 16 hits are detected in 16 successive time windows. The probability of random-noise spikes causing false detection of a signal would thus be about $(1/16)^{16}$ or 5×10^{-20}, which is negligibly small.

The circuit used to achieve this is shown schematically in Fig. 1. For the feedback loop to set the tunnel-diode bias to the correct level, the transmitter is fired at half the rate of the master clock which generates the successive range-gate time windows. Thus, on the interlaced clock pulses when the transmitter does not fire, it is known that no signal can be present and so the 1/16 false-alarm rate can be set. The range gate first resets the tunnel diode D, and any subsequent transition of D which is within the range gate produces a '1' output at the AND gate. After a short time delay τ, successive 1s and 0s are clocked serially into a 32 bit shift register A, which has parallel outputs. These outputs are formed into an analogue sum, amplified, filtered and fed back as a d.c. bias to the tunnel diode in such a sense that the analogue sum on average corresponds to only two 1s being present in the shift register. Changes in ambient noise level at the input to the tunnel diode will simply cause a compensating adjustment in the d.c. bias to maintain the 2/32 false-alarm rate.

On the interleaving pulse train, the transmitter is also fired, and the AND gate is then clocked into a second shift register B. Again, an analogue sum is formed, and is fed into a voltage comparator which causes an alarm when the sum corresponds to greater than, for example, 30 hits following the previous 32 transmitter pulses. Alternatively, very little sensitivity is lost by instead connecting the output of shift register B to a 32 bit AND gate, the alarm criterion then being solely 32/32 hits.

Using a GD 262A germanium tunnel diode, an example of operation of the detector circuit is shown in Fig. 2. In (*a*), a test pulse is shown which is 5 mV in amplitude and about 200 ps wide, and, in (*b*), is shown the resulting circuit waveform at the output of the analogue summer following shift register B. In the left half of the trace is shown the normal 'hunting' in the loop with no input signal present. There are between 0 and a maximum of about 4 hits present in the 32 bit shift register, owing to noise spikes causing the tunnel diode to fire. When the 5 mV pulse train was applied, with a repetition rate around 30 kHz, the analogue sum climbs monotonically to 32 hits. Tests have demonstrated that 5 mV sensitivity is maintained over a temperature range of -18 to $+38°$ C without adjustment to the circuit; at least an order-of-magnitude improvement over open-loop manual setting of the tunnel-diode bias level.

Conclusion: The sensitivity limit of the circuit is determined by the fact that the feedback current is initially quantised before being smoothed by integration in the lowpass filter. Time constants longer than the 1 s used here limit the response rate of the loop to thermal transients. Increased sensitivity is, however, possible by increasing the repetition rate beyond 30 kHz. Alternatively, a wideband video preamplifier can be used to bring the threshold close to the ultimate limit set by thermal noise; using a 26 dB amplifier, we have successfully detected subnanosecond pulses down to 200 μV.

A. M. NICOLSON

Sperry Research Center
Sudbury, Mass., USA

26th May 1977

References

1 NICOLSON, A. M., and ROSS, G. F.: 'A new radar concept for short range application'. IEEE international radar conference, Arlington, Va., April 1975
2 MANTAKAS, CH.: 'Circuit monostable à diode tunnel et dispositif de mise en forme à diode "snap-off"', *Nuclear Inst. & Methods*, 1967, 48, pp. 179–180
3 WHITEHEAD, D. G.: 'Subnanosecond transient detector using emitter-coupled logic gates', *Electron. Lett.*, 1974, 10, 4, pp. 47–48

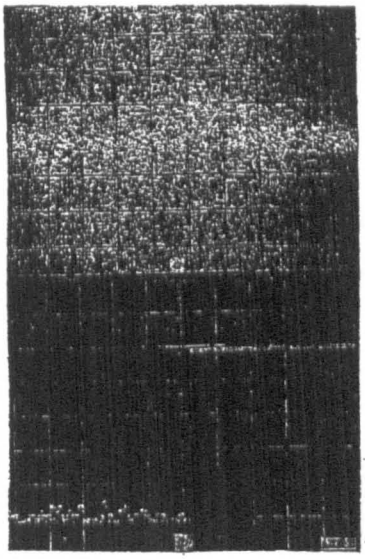


Fig. 2 *Example of operation of the detector using GD262A germanium tunnel diode*

a Input pulse. Vertical scale: 5 mV/division; horizontal scale: 200 ps/division
b Analogue-sum output. Vertical scale: 1 V/division; horizontal scale: 20 ms/division

195

X-BAND TRAPATT AMPLIFIERS

Indexing terms: Microwave amplifiers, Trapatt diodes

A 2-stage, class-C, X-band pulsed trapatt amplifier has been demonstrated, giving a maximum gain of 9·5 dB over a 1 dB bandwidth of 200 MHz at a centre frequency of 9·4 GHz. The trapatt diodes have a silicon p^+–n–n^+ structure with silver integral heatsinks and gold-button heat reservoirs. Single-stage amplifiers have been operated with input pulse widths of 0·5 μs and gains of 5 dB, with 11% 3 dB bandwidths centred at 9·2 GHz.

This letter reports the design and performance of X-band pulsed trapatt amplifiers, and demonstrates the feasibility of cascading two amplifiers to give a net gain of 9·5 dB at a frequency of 9·4 GHz.

The trapatt diodes used in this development may be operated as both oscillators and amplifiers. The structure was fabricated from *n*-type silicon, epitaxially grown, on low-resistivity arsenic-doped substrates. The *n*-type epitaxial layer is phosphorus doped to a level of 7×10^{15} atoms/cm^3 and grown to a thickness of about 3·6 μm. The p^+–n junction is formed by a shallow 40 keV boron-ion implantation of 5×10^{14} ions/cm^3, which is subsequently driven in to produce a graded p^+–n junction with a breakdown voltage of between 30 and 36 V.[1]

The devices were fabricated with silver integral heatsinks (i.h.s.), giving approximately 20% improvement in the steady-state thermal impedance[2] and a marginal improvement in the pulsed thermal impedance relative to the standard gold integral heatsinks. To reduce the transient thermal impedance of the structure, a gold-button heat reservoir was electroplated on the back contact of the diode.[2] The gold button was approximately 35 μm in height, with a thermal time constant of 20 μs, enabling the pulse width of operation to be

extended beyond 5 μs. The steady-state thermal impedance of a diode with a 0·3 pF breakdown capacitance was approximately 40 deg C/W and the thermal impedance over a 5 μs pulse width corresponded to 13 to 15 deg C/W. Larger-area diodes with breakdown capacitances of 0·6 pF gave a steady-state thermal impedance of approximately 30 deg C/W and a thermal impedance over a 5 μs pulse width of 9 to 11 deg C/W.

The trapatt-amplifier circuit consisted of a ruggedised 3·5 mm-diameter 50 Ω coaxial cavity, with an integral bias network. To obtain operation over broad bandwidths with input signal levels of 500 to 600 mW, it was found advantageous to place the filter network close to the diode package,[3] precluding operation in the classical time-domain-triggered (t.d.t.) oscillator mode.[4] The filter consisted of two or three 20 Ω sections between 1 and 4 mm in length. The diode was bonded in an AV162* package, and small changes in the package parasitics could be made by changing the bond-wire configuration, to optimise the amplifier performance. For broad-bandwidth operation with small input signals, a single 0·013 mm-diameter gold wire was bonded between the diode chip and the package. For an oscillator, a 0·025 mm-diameter gold wire bonded from package to chip and back to package gave optimum performance in X-band. Two p.t.f.e. supports were used to hold the inner line concentric; the position of these rings had a considerable influence on both the bandwidth and gain of the amplifier. The cavity could withstand a vibration of 23 g r.m.s. over a spectrum of 10 to 10 000 Hz, without a measurable degradation of the microwave performance of the amplifier parameters.

The amplifier was operated in class-C mode,[1, 2] by applying a d.c. bias below the diode breakdown voltage. A resistance–capacitance network was required in the bias line to absorb the diode voltage dropback as the diode switched into the trapatt mode, and to suppress ringing in the bias circuit. Small diodes of breakdown capacitance of the order of 0·3 pF and operating at a current level of 300 to 400 mA required a bias resistance of approximately 12 Ω. Larger-area diodes of breakdown capacitance 0·6 pF, operating at a current level of 1 A, required a bias resistance of 4 to 5 Ω. Bias-circuit oscillations limited the usable bandwidth; however, they could be greatly reduced by careful design of the bias-circuit network and by including the ferrite bead on the bias line close to the bias-T.

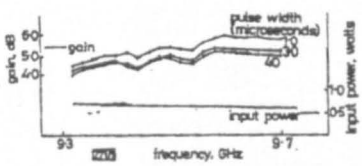


Fig. 1 *Trapatt amplifier with varying input pulse width*

Small-signal reflection trapatt amplifiers used diodes with a breakdown capacitance of 0·25 to 0·35 pF. With input signal levels of 500 to 600 mW and a pulse width of 1 μs and a duty factor of 1%, gains greater than 6 dB with 1 dB bandwidths in excess of 400 MHz have been obtained, at a maximum power added efficiency of approximately 16%. Gains of 8 dB with power added efficiencies of 19% have been observed over a narrower 1 dB bandwidth (170 MHz). Fig. 1 demonstrates the operation of the trapatt amplifier with input signals of 600 mW and pulse widths of between 1 and 4 μs. The Figure shows that there was a maximum drop in gain of 0·75 dB for an increase of pulse width from 1 to 4 μs. Using an Ailtech spectrum analyser with a y.i.g. filter, any out-of-band spurious signals in the frequency range 2·0 to 12·4 GHz were at least 30 dB down on the amplified signal. If the r.f. envelope showed signs of pulse break-up or noise, spurious signals were also observed.

Trapatt amplifiers operating with input pulse widths less than 0·5 μs have demonstrated 11% 3 dB bandwidths centred at 9·2 GHz, with a maximum gain of 5 dB, indicating that the trapatt diodes possess a wide-bandwidth negative resistance.

* Interocram

To obtain a higher overall gain, a cascaded reflection amplifier has been assembled (Fig. 2), using two rugged coaxial cavities. The first stage contained a diode of break-

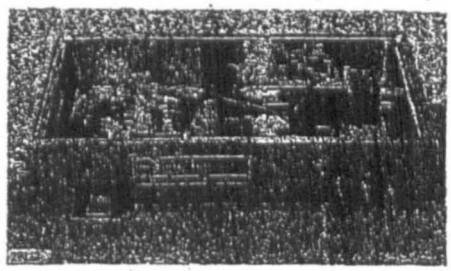


Fig. 2 *Two-stage trapatt amplifier*

down capacitance of approximately 0·3 pF, and the second stage used a larger area device with a breakdown capacitance of 0·6 pF. To reduce feedback between the two stages, a 20 dB isolator was placed between the first and second stage. The amplifier module functioned in a class-C mode, and both stages required ferrite beads on the bias lines to suppress bias-circuit oscillations. The amplifier operated with an input signal level of 550 mW, and, with a 1 μs pulse width at a 1% duty factor, the maximum gain of the module was 9·5 dB over a 1 dB bandwidth of 200 MHz (Fig. 3). The spectrum of the amplified signal was clean, and the first nulls of the $(\sin x/x)^2$ spectrum were 25 to 35 dB below carrier.

Conclusion: The feasibility of exploiting the high efficiency of the silicon p^+–n–n^+ trapatt diode as an X-band amplifier has been demonstrated. Small-signal amplification over

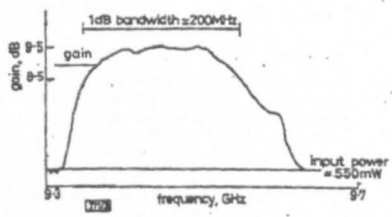


Fig. 3 *Performance of cascaded trapatt amplifier*

1 GHz bandwidths has been achieved, and a cascaded 2-stage circuit has produced output powers in excess of 5 W with 9·5 dB gain. Operation of this amplifier in a class-C mode enables a high overall conversion efficiency to be realised with duty cycles between 8% and single-shot operation.

Acknowledgments: The authors would like to thank S. M. R. Gordon for the fabrication of the trapatt diodes, and I. Mackintosh and R. Royds, R.S.R.E., Malvern, for their advice and contributions. This work has been carried out with the support of the Procurement Executive of the UK Ministry of Defence; it is sponsored by DCVD and is published with the permission of the Directors of The Plessey Company Limited.

C. H. OXLEY
A. M. HOWARD
I. I. PURCELL

Allen Clark Research Centre
The Plessey Company Limited
Caswell, Towcester, Northants, England

14th June 1977

HIGH EFFICIENCY X-BAND TRAPATT AMPLIFIERS AND OSCILLATORS

C.H. Oxley, A.M. Howard, S.M.R. Gordon and J.J. Purcell

ABSTRACT

Silicon p^+nn^+ TRAPATT diodes have given X-band amplification with added power efficiencies of up to 25% and fundamental X-band oscillation with efficiencies as high as 35%. The diodes are fabricated by an Integral Heat Sink (IHS) technology and the p^+n junction is formed by a combination of ion implantation and a drive-in period. Double-sided heat sinking has enabled oscillator performance to be extended to pulse-widths of greater than 5 microseconds, and mean output powers of 1 Watt have been recorded. Coaxial amplifier circuits produced small signal gains of 9dB, and large signal gains of 4dB with 1dB bandwidths of 500 MHz at 9.25 GHz with RF peak powers of over 12 watts. The design and performance of both coaxial and microstrip circuits is discussed.

INTRODUCTION

The TRAPATT diode offers considerable potential for X-band air-borne transponders and medium range radar applications, where high efficiency and pulse versatility is required.

Silicon p^+nn^+ TRAPATT diodes have been operated as X-band oscillators with efficiencies as great as 35% with peak powers of 15 watts and have given X-band amplification with efficiencies up to 25%.

FABRICATION

The diodes are fabricated from n-type silicon epitaxially grown on low resistivity arsenic-doped substrates. The epitaxial layer is phosphorus doped to a level of about 7×10^{15} atoms/cm^3 and is grown to a thickness of approximately 3.6 microns. The p^+n junction is formed by a shallow, 40KeV, boron ion implantation dose of 5×10^{14} ions/cm^2, which is subsequently driven in approximately 3.3 microns to produce a graded p^+n interface (1). For optimum X-band performance, diodes were found to have an effective active layer width of 0.2 - 0.4 microns, as estimated by an optical interference method (2,3), and a breakdown voltage of 28-36 Volts.

All diodes were fabricated by an Integral Heat Sink (IHS) process, in which a gold heat sink is electroplated on to the junction side of the slice. Typical steady state thermal impedance values were 50-37°C/W, for packaged X-band diodes with breakdown capacitances in the range of 0.3 - 0.6 pF.

To reduce the transient thermal impedance of the structure, a gold heat reservoir 'button' was electro-plated on the top-contact of the diode (4). This effectively reduced the thermal impedance over short pulse widths (1-5 microseconds); as heat could be extracted from both sides of the junction. For long pulse widths the thermal impedance becomes asymptotic to the steady state value.

Allen Clark Research Centre, Plessey Co. Ltd., Caswell, Towcester, Northants.

CIRCUITS

Coaxial Circuit

A 3.5mm diameter slotted 50 Ohm coaxial air line*, has supported efficient fundamental TRAPATT oscillations to frequencies as high as 10 GHz.

Three 6-10 Ohm anodised tuning slugs were used to establish the appropriate filter characteristics. The distance between the first slug and the diode plane was slightly less than a half-wavelength of the fundamental frequency. It was found that a lumped capacitance, in the form of a PTFE slug, placed in the air-line, around the diode, resulted in a considerable increase in microwave performance, as previously reported (1 and 5). The diodes were bonded into AY-162* packages.

Figures 1 and 2 summarise the efficiencies and peak powers as a function of frequency obtained in this laboratory to date. These results were obtained with pulse-widths of about 0.5 microseconds and duty factors of approximately 0.1%. The X-band performance followed a well behaved pattern of an approximately constant efficiency and a linearly increasing peak power with increasing bias current. Most diodes performed with a clean rf envelope with rise times of the order of 30-40 nanoseconds and frequency chirps of approximately 100 MHz. Diodes which gave efficiencies of 30% with peak powers of greater than 10 Watts in X-band, had breakdown voltages and capacitances in the range of 28-34 Volts and 0.3-0.5 pF respectively.

The points on figures 1 and 2 depicting high frequency operation (J-band) were obtained by harmonic extraction (6). To obtain harmonic operation the tuning slugs were re-adjusted in order to load the required harmonic resistively, and the fundamental and other harmonics reactively.

An 80 micron diode processed by the IBS technique, and having a gold heat reservoir, produced a pulsed thermal impedance value of approximately 71° C/W over a 5 microsecond pulse-width, and a steady state thermal impedance of approximately 37° C/W, enabling long pulse and high duty factor operation. Typical results are summarised in Table 1. These include mean powers of 1 Watt for pulse-widths of 0.4 microsecond and duty factors of 8:1.

MICROSTRIP OSCILLATOR

Systems requirements for low cost, rugged modules indicate the potential advantages of a TRAPATT source utilising a microstrip circuit.

Computer analysis has shown that the relative position of the slugs in the TRAPATT coaxial cavity do not equate to those of a simple maximally flat or Chebyshev low-pass filter. The network appears to be complicated, with the first slug acting as a impedance transformer at the fundamental frequency and the other tuning elements providing the required reactive loading at the harmonics.

TABLE 1

Duty Factor (%)	Pulse Width (microsecs)	Mean Power (mW)	Efficiency (%)
10	0.5	850	32
13	0.4	1000	26
16	0.4	1100	23
8	3.0	620	24
4	3.0	185	27
10	5.0	580	20

Owing to the difficulty of analysing the TRAPATT cavity, a direct equivalent of the coaxial cavity was made on microstrip. A 10 thou thick alumina substrate was used to facilitate the realization of the low impedance sections of approximately 10 Ohms. The diode was bonded in an AV-162 package which was mounted coaxially with the microstrip circuit. In general, two additional matching elements were required; a high permittivity zirconate chip placed close to the diode package, and a small metal disc of diameter 30 thou mounted on the 50 Ohm line after the filter network. The zirconate chip appeared to reactively match the circuit impedance to that of the packaged diode at the fundamental frequency of operation. The electrical distance between the diode and the filter plane was approximately a half wave length at the fundamental frequency of operation. The small metal disc on the 50 Ohm line influences the resistive load at the package plane. Diodes from a number of layers, having a range of capacitances 0.3-0.7 pF have been operated as oscillators over the frequency range of 7.0 to 9.0 GHz. Peak powers of approximately 9 Watts and efficiencies of approximately 20% have been recorded at 7.0 GHz. As with the coaxial circuit, the microstrip circuit demonstrated a fairly constant efficiency and a linearly increasing peak power with increasing bias current (Fig. 3), for a 0.5 microsecond pulse-width at 0.1% duty factor.

AMPLIFIERS

Coaxial Circuit

The Amplifier circuit consisted of the 3.5 mm diameter air-line oscillator circuit with the low impedance (7-10 Ohm) tuning slugs re-adjusted slightly. The diode chips were mounted in AV-162 packages and positioned at a little less than half the fundamental wavelength from the filter plane.

The TRAPATT amplifier circuit was biased for Class C operation, by applying a dc bias just below the breakdown voltage of the diode (7). A resistive-capacitive network was required in the bias-line to absorb the diode voltage drop-back.

Small area diodes with a breakdown capacitance of approximately 0.3-0.4 pF have given amplifier added power efficiencies as high as 25% in X-band. These diodes gave dc to rf conversion efficiencies of 30% as oscillators in X-band.

Under small signal operation with approximately 1.25 Watts input power with a pulse-width of 0.5 microseconds and 0.1% duty factor, a gain of up to 7 dB with a 1 dB bandwidth of 280 MHz (Fig. 4) at a centre frequency of 9.15 GHz has been observed. Small signal gains of 9 dB have been observed with a bandwidth reduced to approximately 150 MHz. Figure 5 demonstrates a large signal bandwidth of 545 MHz at a centre frequency of 9.25 GHz and a gain of 3-4 dB.

Large signal coaxial amplifiers giving a gain of 4-5 dB have been operated over a temperature range of 20-70°C. A 1 dB variation in gain with temperature was observed. A constant gain of between 4 and 5 dB could be maintained over the 50°C temperature range, by increasing the bias voltage by approximately 6%.

Microstrip Circuit

Microstrip amplifier operation has been obtained. This has been accomplished by using a microstrip oscillator circuit, with a different tuning arrangement. The metal disc was replaced by a second dielectric zirconate chip. This had the effect of raising the magnitude of the resistive component seen by the package and diode. Diodes of 0.6 pF have demonstrated gains of 4-5 dB with peak powers of 10 Watts and 1 dB bandwidths of approximately 300 MHz at a centre frequency of 9.25 GHz with a power added efficiency of 16% for a 0.5 microsecond pulse width. A typical result is shown in Fig. 6, operating at a centre frequency of 8.9 GHz.

REFERENCES

1. J.J. Purcell, M.R. Weatherhead, S.M.R. Gordon, C.H. Oxley and P.R. Wickens, 'High Efficiency TRAPATT Operation in X-band', Electronic Letters Vol. 11, No.11, pp. 236-238, May 1975.

2. R.W. Bicknell, 'A Simple Rotating Jet-Thinning Apparatus for Producing Taper Sections and Electron Microscope Specimens from Silicon and Compound Semiconductors', J. Physics D. 1973, 6, pp. 1991-1997.

3. A.M. Howard, D.J. Smith, J.J. Purcell 'Epitaxially grown Double Drift Silicon Impatt Diodes at 60 to 90 GHz', Elec. Letts. 17th Oct. 1974, Vol. 10, No. 21.

4. W.R. Curtice, J.J. Risko, and P.T. Ho, 'A Study of Second Harmonic-Extraction TRAPATT Amplifiers for X-Band Operation', RCA Review, Vol. 36, June 1975.

5. W.J. Evans, 'Circuits for High Efficiency Avalanche Diode Oscillators', IEEE Trans. 1969, MTT-17, pp. 1060-1067.

6. N.A. Slaymaker, J.E. Carroll, 'Efficient Power Extraction at TRAPATT Harmonics', Elec. Letts. November 1970, Vol. 6, No. 23.

7. A. Rosen, J.E. Reynolds, S.L. Liu and S.G. Theriault, 'Wideband Class C TRAPATT Amplifiers', RCA Review, Vol. 33, December 1972.

*manufactured by RSRE (Malvern) U.K. † Interocean.

160

FIG. 1

EXPERIMENTALLY OBSERVED EFFICIENCIES OF PULSED SILICON TRAPATT DIODES

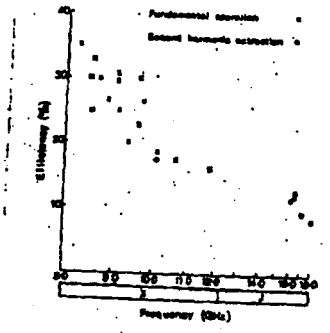


FIG. 2

EXPERIMENTALLY OBSERVED RF POWERS OF PULSED SILICON TRAPATT DIODES

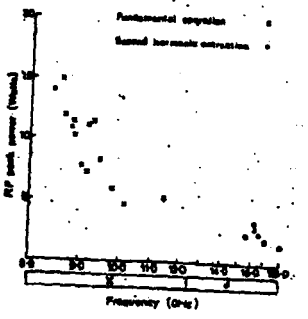


FIG. 3

MICROSTRIP OSCILLATOR

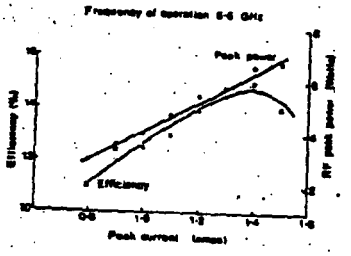


FIG. 4

SMALL SIGNAL BANDWIDTH

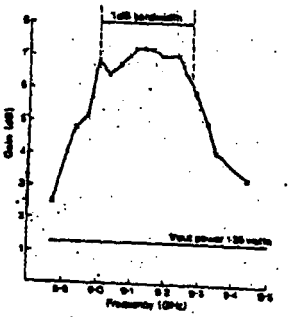


FIG. 5

LARGE SIGNAL BANDWIDTH

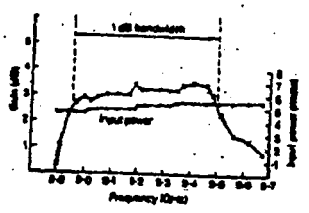
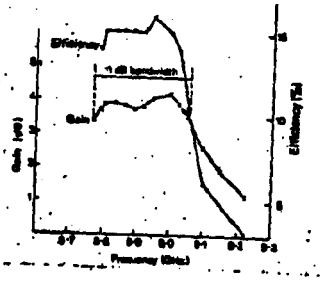


FIG. 6

MICROSTRIP AMPLIFIER



Design and performance of trapatt devices, oscillators and amplifiers

C. H. Oxley, A. M. Howard and J. J. Purcell

Indexing terms; Microwave amplifiers, Microwave oscillators, Semiconductor diodes, Solid-state microwave devices, Transit-time devices

Abstract: Silicon p^+nn^+ trapatt diodes have been fabricated by integral-heat-sink (t.h.s.) technology. The graded p^+n junction has been formed by two methods; by deposition and by a low energy implantation, both of which were followed by a drive-in period. Oscillator efficiencies of 55% in L-band, and 35% in X-band were recorded. R.F. peak powers of up to 15 W in X-band have been observed. J-band operation has been obtained by 2nd-harmonic extraction, giving efficiencies of 19% to 16 GHz. Low steady-state thermal impedance has enabled operation with mean powers in excess of 1 W in X-band. Diodes with improved transient thermal impedance have enabled operation to be extended beyond 5 μs pulsewidth. Coaxial amplifier circuits produced small-signal gains of 9 dB and added-power efficiencies of 25% at 9 GHz. Large-signal gains of 4 dB with 1 dB bandwidths of 500 MHz with r.f. peak powers of over 12 W have been obtained. Amplifiers have been operated with a 1 dB variation in gain over a temperature range of 50 deg C.

1 Introduction

The trapatt mode was discovered in 1967 by Prager, Chang and Weisbrod.[1] It has permitted the realisation of high-efficiency solid-state microwave oscillators and amplifiers. D.C.-r.f. conversion efficiencies as high as 60% are obtained at frequencies of 1–2 GHz, and several authors[2,3] have reported efficiencies as high as 35% at X-band frequencies.

The ideal profile for a conventional p^+nn^+ trapatt diode consists of a narrow active-region width of doping density n, with abrupt p^+n and nn^+ interfaces. This structure is heavily 'punchthrough' at breakdown, unlike the impatt diode. In practical trapatt diodes, punchthrough factors F can approach values of up to 6, where

$$F = \left(\frac{V_B}{V_P}\right)^{1/2}$$

V_B = breakdown voltage of the nonpunchthrough diode of same doping level;

V_P = punchthrough voltage.

Trapatt action occurs when a rapidly increasing reverse-bias voltage of magnitude greater than the breakdown voltage is applied across the depleted diode. An avalanche zone sweeps rapidly from the junction, through the depletion layer to the substrate, leaving in its wake a dense plasma of holes and electrons and collapsing the electric field. The diode drops into a low-voltage high-current state, and the carriers are said to be trapped, as their drift velocities fall well below their saturated values. As the carriers drift slowly out of the active region under low-field conditions, the electric field within the diode recovers. When the electric field has fully recovered and the current returns to essentially zero, the cycle is repeated. The current and voltage waveforms produced are favourable to the production of high efficiencies. The frequency of operation is much lower than in the impatt mode, since the carriers spend a long part of the cycle with drift velocities well below the saturated drift velocity.

In practice, it has been found that trapatt devices with abrupt junctions were prone to premature burn-out. Graded p^+n interfaces have enabled higher current densities to be tolerated, with consequent improvements in maximum powers and efficiencies.

2 Device fabrication

Practical realisation of the device design goals may be achieved, to a degree, by using techniques common to most high-frequency solid-state devices; however, certain aspects require special attention in the trapatt diode. To minimise series parasitic resistance, and to ensure a low-resistance ohmic contact to devices, it is preferable to use heavily doped, low-resistivity substrate material, especially in the case of small-area high-frequency diodes. An impurity concentration of 5×10^{19} atoms/cm^3 (0·001 5 Ωcm) is achievable using arsenic-doped silicon substrates, but precautions have to be taken to prevent the escape of this highly volatile element during any high-temperature treatment of the material.

For optimum device performance, the trapatt specification demands a high degree of control of the n-region doping level and thickness. Growth by the silane epitaxial process has been chosen at Caswell because it facilitates precise doping and thickness control and may be performed at a relatively low temperature (1075°C), thus minimising n/n^+ interface degradation during growth. Before growth of the epitaxial layer, a coating of silicon dioxide is grown at high temperature in steam over the substrate surfaces. A window is then etched through the oxide where the phosphorus-doped n-layer growth is required, the remaining

Paper T16, first received 24 May and in revised form 23rd June 1976

The authors are with the Allen Clark Research Centre, The Plessey Company Limited, Caswell, Towcester, Northants NN12 8EQ, England

162

oxide preventing the escape of arsenic, which would otherwise contribute to the epitaxial layer doping during its growth.

After growth, the *n*-region doping concentration is measured using an automatic profiler[4] in conjunction with a mercury Schottky-barrier diode made to the surface of the layer. As the *n*-type active-region width of the trapatt structure constitutes only a small proportion (typically one-seventh) of the total *n*-layer grown, a very accurate total-thickness measurement method is required to obtain an acceptable active-region-width assessment. For example, a tolerance of ± 25% on the active-region width requires a tolerance of approximately ± 5% on the total *n*-layer thickness. The procedure employed at Caswell is the jet etch and stain method,[5] which uses an interference technique to measure the *n*-layer thickness. A hemispherical hole is etched through the layer from the substrate side (Fig. 1) to form a small angle bevel at the epitaxial side. On immersing the specimen in copper-sulphate solution, preferential copper plating of the n^+ substrate takes place, so defining the extent of the epitaxial region. Under sodium-light illumination, fringes are formed at the surface of the specimen resulting from interference between directly reflected light and light reflected internally from the epitaxial surface through the semiconductor. The half-wavelength of sodium light in silicon is 750 Å, which corresponds to the fringe spacing observed. Determination of the epitaxial-layer thickness is then simply a question of counting the fringes to the point at which the copper plating commences and multiplying this number by 750 Å.

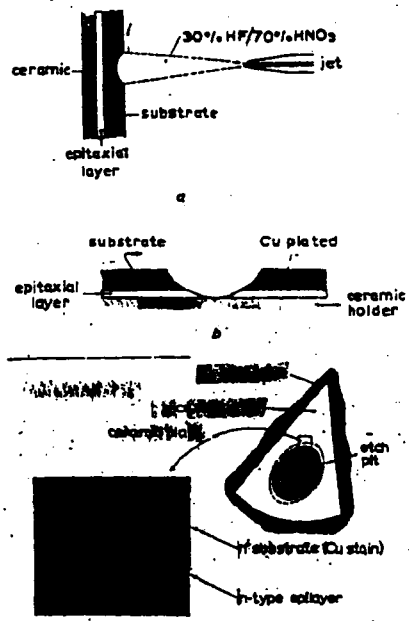


Fig. 1 *Trapatt diode structure*
a Jet etching technique
b Profile of etch pit after decoration
c *n*- on n^+ slice

For a typical X-band trapatt structure with a total *n*-layer width of about 3·5 μm, this gives a resolution of approximately 2%.

Formation of the graded *pn* junction requires deposition of a source of acceptor impurity atoms, followed by a thermally accelerated diffusion stage to drive them into the *n*-type epitaxial layer. In the authors' laboratory, the source of acceptors is provided by implanting low-energy boron ions into the surface of the *n*-region; however, deposition from an oxidised-boron-nitride source has also been satisfactorily used. To reduce the length of time taken to drive the boron into the *n*-layer, and thus minimise the degradation of the n/n^+ interface, the drive-in may be performed in a nitrogen atmosphere with a small percentage of oxygen added to enhance the boron diffusion rate. The drive-in process depletes the layer surface of acceptors; thus it is necessary to replenish this region with a further deposition of boron to ensure a low-resistance ohmic contact to the semiconductor. A 30 min deposition from an oxidised-boron-nitride source at 860°C adequately satisfies this requirement without significant degradation of the doping profile. It is possible to compensate for material which departs slightly from the required epitaxial-layer specification by making small adjustments to the drive-in time, and hence the active-region width, without significantly changing the shape of the impurity profile.

To assess fully the completed trapatt slice, 'surface diodes' are made on a specimen of the layer. The epitaxial side of the layer is metallised, and circular contacts are formed by standard photolithographic techniques. Mesas are then etched in the semiconductor using the metal contacts as masks. The contacts are then reduced in size to allow a visual measurement of the junction area to be made, which, with a determination of the reverse-bias junction capacitance, enables the capacitance per unit area to be determined. The quality and magnitude of the reverse-bias breakdown may also be obtained from tests made on these diodes.

The fabrication technique used in the production of trapatt devices is largely determined by consideration of their thermal impedance. The 'integral heatsink' (i.h.s.) fabrication procedure, used successfully for many other microwave devices, has been adopted by the authors. The first stage is to metallise (by evaporation or sputtering) the epitaxial side of the material, forming an electrical contact metal, such as titanium or chromium, which adheres which to plate the heatsink. The metallisation consists of a contact metal, such as titanium or chromium, which adhere well to the semiconductor, followed by a refractory metal such as palladium or platinum onto which the heatsink is plated. Gold is usually chosen for the heatsink because of its high thermal conductivity, resistance to corrosion and the ease with which it can be bonded to device packages.

After the heatsink has been plated, the semiconductor substrate is thinned by lapping and etching, and contact is made to it using the same metallisation as for the epitaxial side. Standard photolithographic procedures are used to define metal dots on the substrate metallisation, these in turn being used as masks to mesa etch the semiconductor right through to the metallisation on the epitaxial side. Use of the capacitance-per-unit-area information determined from surface diodes allows the selection of the appropriate dot area corresponding to the desired device capacitance. The completed batch of diodes is then separated into discrete devices by cutting through the gold heatsink

between the rows of mesas (Fig. 2). These are then individually ultrasonically bonded into packages suitable for microwave operation, and a wire or tape is bonded to the substrate contact to form the second terminal of the device.

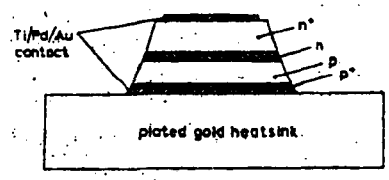


Fig. 2 *Integral heat-sink structure*

3 Device thermal considerations

Heat generated in the active region of a pulsed trapatt diode initially flows into both the substrate and into the heatsink. The substrate region temperature rises to approximately that of the active region, and, from then on, the heat flows only in the direction of the plated heatsink. Consequently, the effective thermal impedance of a device for short pulses can be much less than the steady-state value approached with increasingly longer pulses. Provided that the time between pulses is long enough, the device cools almost to the ambient temperature after each pulse. However, as the duty factor is increased, significant mean heating occurs, and the device assumes a mean temperature greater than that of its environment.

By the connection of two devices in parallel in the same package, the steady-state thermal impedance may be reduced by a factor approaching $1/\sqrt{2}$ of that of a single device with the same total area. For a given set of bias conditions, this, or any other reduction in the steady-state thermal impedance, leads to both a reduction in the temperature rise across a pulse and a reduction in the mean operation temperature.

For very short pulses, the heat flow from the active region is the same into both the epitaxial and substrate semiconductor regions, the effective thermal impedance being approximately one-half the steady-state value. By the addition of a heat reservoir (Fig. 3) to the substrate side of the device, longer pulses may be applied within the 'half-thermal-impedance' limitation.[6] Optimum utilisation of this effect is realised only if the substrate is reduced during fabrication to a thickness no greater than that of the epitaxial region. The reservoir may be produced by plating a gold 'button' onto the substrate metallisation.

Parallel-mounted devices, and devices with gold buttons, have both been produced in the authors' laboratories with improvements in performance close to those predicted by theory.

4 Circuit description

The trapatt circuit usually comprises a 50 Ω coaxial airline with a low-pass filter situated just less than half the fundamental wavelength from the diode plane. At the trapatt frequency, looking into the circuit from the diode plane, the circuit has a reactive and a capacitive component. At harmonics of the trapatt frequency, the circuit is equivalent to a short-circuited line. When the trapatt pulse is initiated, the diode voltage collapses approximately to zero, and a negative-going voltage pulse propagates along the line to be reflected from the filter plane as a positive-going pulse. The positive voltage pulse then provides the overvoltage required to trigger the next trapatt cycle. The time of transit of the voltage pulse from the diode to the filter determines the trapatt frequency. This cyclical triggering mechanism is known as time-domain triggering (t.d.t.) and was first realised by Evans.[7]

The trapatt waveform is rich in harmonics, which are important to the efficient operation of the trapatt diode. The standard trapatt coaxial cavity is a 7 mm-diameter 50 Ω air line, and the normal coaxial propagation mode is the TEM. Higher-order modes are supported above a frequency of approximately 20 GHz. It was observed that, on tuning an efficient trapatt oscillator in the 1–2 GHz range and inserting a capacitive probe into the circuit between the diode and the filter, frequencies up to and including the fifth harmonic could be detected. The relative importance of the harmonics to the operation of the trapatt diode probably decreases with increasing harmonic number.[8] Experimentally it was observed that efficient trapatt operation in the 7 mm line could be obtained at fundamental frequencies below about 5 GHz. Higher-frequency operation resulted in reduced efficiencies, accompanied by the absence of the higher harmonics. A 3·5 mm-diameter 50 Ω coaxial airline is single-moded to approximately 40 GHz. It was found that a circuit based on this airline* enabled efficient trapatt operation to be extended to frequencies as high as 10 GHz.

The 3·5 mm line has a 1 mm-wide slot milled along its length to provide access to the tuning slugs, and the line is gold-plated to minimise skin-effect losses.

Three 10 Ω anodised tuning slugs were used to establish the appropriate filter characteristics. The tuning slugs were between 1·0 and 3·5 mm in length, and the exact lengths and configurations used depended upon the diode and package impedance and the frequency of operation. The distance between the first slug and the diode plane was slightly less than a halfwavelength of the fundamental frequency.

It was found that a lumped capacitance, in the form of a p.t.f.e. slug, placed in the airline around the diode, resulted in a considerable increase in microwave performance as previously reported.[2,7] The p.t.f.e. probably serves two functions, namely it provides extra capacitance in the line to supply charge at the instant the voltage across the diode collapses,[9] and secondly it acts as a matching element to the packaged diode. Optimum microwave performance between 8·4 and 9·0 GHz required an extra lumped capacitance of approximately 1·0 pF, whereas for frequencies of

* Manufactured at the RSRE, Malvern, England

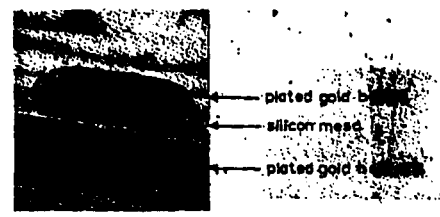


Fig. 3 *Trapatt diode with heatsink button*

164

operation above 10 GHz, about 0·6 pF of lumped capacitance was used.

Two small p.t.f.e. discs were included between the filter network and the bias tee. These had considerable influence on the operation of the oscillator. Measurements using the network analyser suggested that the relative positions of the discs provided small changes in the fundamental phase which were found to effect significant improvements in the r.f. performance.

For low-frequency operation, between 1 and 4 GHz, diodes were bonded into S-4 packages. The S-4 package is restricted to low-frequency trapatt operation, as the magnitude of the parasitic reactances adversely affects the higher-frequency content of the trapatt waveform. For X-band operation, the AV-162† package, which has a much higher cut-off frequency, was used. Experimental evidence suggests that the oscillator operated with comparable powers and efficiencies with different types of bonding configurations in the AV-162 package; for example, tapes, 0·001 in-diameter wire, and 0·0005 in-diameter wire.

5 Microwave performance

The trapatt diode offers a high versatility to the system engineer, as it operates with high efficiency and high peak powers, long pulsewidths and high duty factors, and diodes may be operated as t.d.t. oscillators, frequency-locked oscillators and reflection amplifiers.

The curves in Figs. 4 and 5 demonstrate the efficiencies and peak powers as a function of frequency, obtained in this laboratory to date. Both curves show an inverse dependence on frequency. A 7 mm-diameter coaxial circuit was used for frequencies below 5 GHz, and the 3·5 mm-diameter coaxial circuit was used at higher frequencies. These results were obtained with pulsewidths of about 0·5 μs and duty factors of approximately 0·1%. The X-band performance followed a well behaved pattern of a fairly flat efficiency curve and a linearly increasing peak power with increasing bias current (Fig. 6). The maximum efficiency generally occurred at a current density of approximately $1·2 \times 10^4$ A/cm^2. Typically, all diodes gave a clean r.f. envelope with risetimes of the order of 30–40 ns. Diodes that gave efficiencies of 30%, with pulse-peak powers of greater than 10 W in X-band had breakdown voltages and capacitances in the ranges 28–34 V and 0·3–0·5 pF, respectively. As the capacitance of the diode increased above 0·6 pF, matching to the circuit became more difficult and the efficiency was reduced.

The points on the curves demonstrating higher-frequency operation (J-band) were obtained by harmonic-extraction techniques.[18] This reduced the complexity of both fabricating high-frequency trapatt diodes and constructing a high-frequency coaxial circuit.

To obtain harmonic extraction in the 3·5 mm-diameter coaxial line, the tuning slugs were retuned in order to load the required harmonic resistively, while terminating funda-

† Interwave

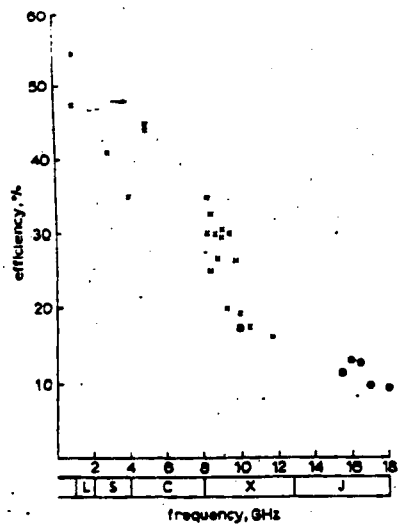


Fig. 4 *Experimentally observed efficiencies of pulsed silicon trapatt diodes*

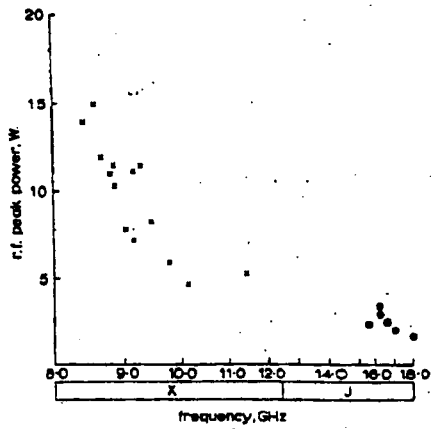


Fig. 5 *Experimentally observed r.f. powers of pulsed silicon trapatt diodes*

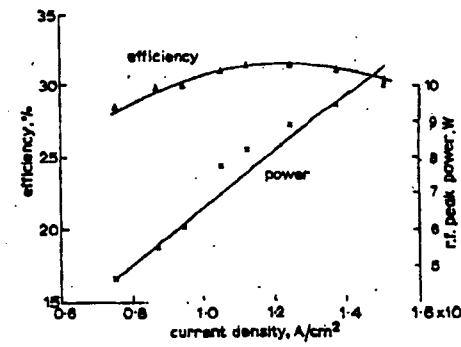


Fig. 6 *Pulse peak power and efficiency versus current density*

165

mental and other harmonics reactively. It was found to be advantageous to make the first slug of the filter less than 1·0 mm in length, and this was placed at approximately half the fundamental wavelength from the diode plane. Diodes which performed with maximum efficiency of 12–13% in the J-band, had breakdown voltages between 28–26 V and breakdown capacitances of less than 0·4 pF. At present, the smaller size of the diodes, and efficiencies of 13%, have restricted peak powers to the order of 3·5 W at 16–17 GHz.

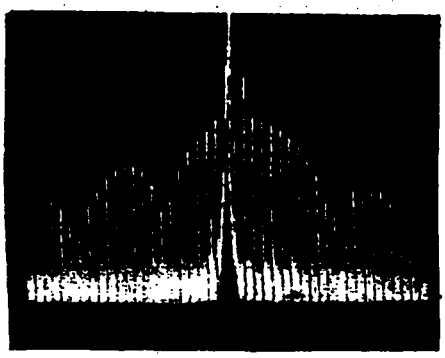


Fig. 7 Frequency locked TRAPATT oscillator

Centre frequency = 9·0 GHz
Dispersion 1 MHz/div; vertical displacement 10 dB/div

It is a well known phenomenon that a stable high-powered and narrowband source may be obtained, by frequency locking the source to a more stable low-powered c.w. source. As the frequency spectrum of the trapatt diode is relatively wide, for example an X-band source operating with a 400 ns pulsewidth at 1% duty factor exhibits a frequency dispersion of approximately 100 MHz, frequency-locked operation may be advantageous. An X-band trapatt pulsed oscillator has been successfully frequency locked with a c.w. X-band Gunn source, with a locking power of 100–300 mW. The locked trapatt oscillator was well behaved and could be pulled through a bandwidth of 100 MHz by the Gunn locking source. Typical locking power gains, for a 400 μs pulsewidth at a centre frequency of 9·0 GHz with 5·0 W of locked-oscillator power, were of the order of 12 dB. Fig. 7 demonstrates the much improved frequency spectrum of the locked trapatt source, with the first null approximately 25 dB down on the centre-lobe. The spectrum was additionally improved by passing a continuous current of a few milliamperes through the diode.[12]

With the conventional i.h.s. diode structure, pulsewidths of 1–1·5 μs could be obtained with input powers of the order of 25–30 W before the r.f. envelope started to break up. At the point of pulse break-up, the estimated junction temperature was approximately 260°C. Extended pulse operation was attained by extracting heat from both sides of the junction by means of a gold-button heatsink on the top contact, as previously described. This enabled diodes to be operated with input powers of 25 W with clean detected r.f. envelopes of greater than 5 μs pulsewidth.

Using the gold-button diode structure described and an input power of the order of 20–25 W, 20 μs pulsewidth operation has been obtained with an efficiency of 18–16% and an r.f. peak power of 4–5 W, with a frequency chirp across the pulsewidth of the order of 300 MHz. It was observed that, for pulsewidths greater than 1 μs, the frequency chirp showed a similar response to pulsewidth as that of the theoretical temperature rise of the gold-button heat reservoir. The temperature response of the gold button may be approximated by the expression[13]

$$\frac{T}{T_0} = 1 - \exp\left(\frac{-t\alpha}{l^2}\right)$$

where

T = temperature of button reservoir
T_0 = temperature of junction
l = thickness of button heat reservoir (approximately 35 μm)
α = diffusivity of gold (1·18 cm²/sec)
t = pulsewidth, μs.

Short-pulse operation, with pulsewidths of approximately 0·5 μs in the X-band gave frequency chirps of the order of 100 MHz, which appeared to be almost independent of the thermal impedance of the diode.

Frequency-pushing values of 30–40 MHz/100 mA were obtained for a typical X-band trapatt diode operating with a 0·4 μs pulsewidth and 0·5% duty factor. The pushing magnitude shows that current-bias pulse shaping is not a practical solution for correcting the observed frequency chirps of 100–300 MHz over pulsewidths of 0·5–20·0 μs.

For certain radar applications, high mean power is required. The conventional i.h.s. trapatt structure with a c.w. thermal impedance of the order of 30–40 deg C/W is incapable of dissipating the high mean d.c. power associated with c.w. trapatt operation but is quite capable of dissipating 3–4 W of mean power. Hence trapatt operation with narrow pulsewidths (0·4–0·5 μs) and high duty factors are quite feasible. Diodes have been operated at up to 15% duty factor, the maximum duty factor being limited by the pulse modulator. Mean powers of over 1·1 W in the frequency range of 8·5–9·0 GHz and efficiencies of 23–26% have been observed.

A combination of the gold-button structure and the conventional i.h.s. structure has led to the operation of diodes with long pulsewidths and high duty factors with junction temperatures of the order of 260–280°C. Results obtained to date are summarised in Table 1.

Table 1

Duty factor	Pulsewidth	Mean power	Efficiency
%	μs	mW	%
10	0·5	850	32
8	3·0	520	24
4	3·0	185	27
10	5·0	580	20
13	0·4	1000	26
16	0·4	1100	23
1	20·0	45	16

To improve further the steady-state thermal impedance of the trapatt structure for operation with long pulsewidth and high duty factor, at a lower junction temperature, a preliminary investigation into parallel connection of diodes has been made. The r.f. performance of this structure, in X-band, has been encouraging. When two diodes of similar size and breakdown capacitance are tightly coupled elec-

166

trically, by means of a 0·001 in bond-wire, 90% power addition, with similar overall efficiencies, is obtained compared with the single diode, and the overall steady-state thermal impedance is reduced by 20%. For example, a single diode gave 2·5 W r.f. pulsed power at an efficiency of 24–25%, and two similar diodes coupled together gave 4·75 W of peak power with an efficiency of 25%.

Good reproducibility of diodes from slice to slice has been experienced. From six silicon slices processed, four slices have given batches of diodes performing with efficiencies of 30% in X-band. Of a particular slice from which a batch of 21 devices were chosen, with a breakdown capacitance of 0·3 to 0·5 pF, more than one-third had an efficiency greater than 30% and more than half delivered powers in excess of 10 W.

6 Trapatt amplifier

Fundamental X-band trapatt reflection amplification has been observed using both coaxial and microstrip circuits.

The amplifier circuit consisted of the t.d.t.-oscillator coaxial stripline, with a slight modification to the positions of the tuning slugs to obtain a small-signal-stable amplified signal. The diodes were bonded in an AV-162 package with a single 0·001 in gold wire, and the package positioned at a little less than half a wavelength from the filter plane.

The trapatt amplifier circuit was biased for class-C operation, in which the trapatt diode is held just below its breakdown voltage. In this state, the diode is in effect switched off, as negligible current flows through it. When an r.f. signal of sufficient amplitude is applied, the trapatt mode is triggered, the voltage drops below the bias voltage, a large current flows through the diode, and r.f. amplification occurs. In the absence of the r.f. signal, the diode returns to its off state, and little current flows.[13] Biasing the diode below the breakdown voltage was achieved by two approaches. Either by using a pulse generator that provided a voltage pulse just below the breakdown of the diode, which was synchronised to the generator driving the r.f. input source — a high-powered pulsed X-band Gunn diode; or by applying a d.c. bias just below the breakdown voltage of the diode. In the latter approach, a resistance-capacitance network was required in the bias line to absorb the diode voltage dropback.

The S_{11} parameters at the diode package plane for both amplifier and t.d.t.-oscillator circuits were measured between 8 and 12 GHz on a network analyser. The measurements showed that the amplifier circuit was loaded at the fundamental frequency by a real impedance of approximately 15–20 Ω, compared with 5–8 Ω for the t.d.t.-oscillator circuit. The measurement suggests that the amplifier circuit may be more easily realised than the t.d.t.-oscillator circuit, and that larger-area diodes should be more easily matched in an amplifier than in an oscillator.

Experimentally, larger diodes with breakdown capacitances greater than 0·7 pF appeared to be more readily matched in the amplifier circuit than in the oscillator circuit. Smaller-area diodes, with a breakdown capacitance of approximately 0·3–0·4 pF, have given device-amplifier added-power efficiencies as high as 25% in X-band.

Under small-signal operation with approximately 1·25 W input power with a pulsewidth of 0·5 μs and 0·1% duty factor, gains of up to 7 dB with 1 dB bandwidth of 280 MHz (Fig. 8) at a centre frequency of 9·15 GHz have been observed. Small-signal gains up to 9 dB have also been observed, but with much reduced bandwidths. Under large-signal operation, gain compression occurs with increased bandwidth. Fig. 9 shows a 1 dB bandwidth of approximately 545 MHz at a centre frequency of 9·25 GHz with a gain of 3–4 dB, for an input signal of 5 W. There was very little distortion in the output spectrum compared with the input spectrum at several spot frequencies across the passband.

A large-signal amplifier giving a gain of 4 dB has been operated over a temperature range of 20—70°C, which resulted in a maximum variation of 1 dB of gain. Measurements have shown that, by gradually increasing the bias voltage by a maximum of a few volts as the temperature is increased from 20 to 70°C, a constant gain of 4 dB can be maintained. Hence trapatt amplification with constant gain over a 50 deg C temperature range is obtainable.

7 Conclusion

The development of both diode fabrication and circuit techniques has resulted in the demonstration of efficient high-power trapatt performance over the frequency range 1—10 GHz.

X-band efficiencies in excess of 30% have been reproducibly achieved, indicating the potential of trapatt devices in airborne transponders and medium-range radar systems.

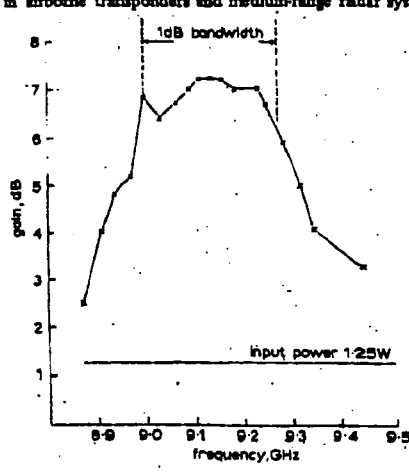


Fig. 8 *Small-signal bandwidth*

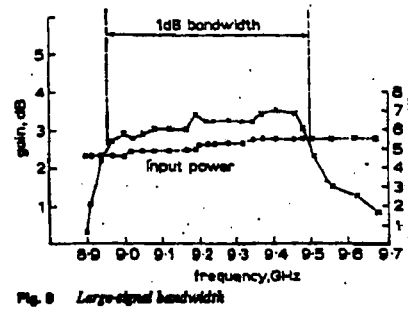


Fig. 9 *Large-signal bandwidth*

167

X-band amplifiers have been tested and shown to be stable with realistic variations in ambient temperature and bias conditions. Operation in a 'class-C' permits overall added-power efficiencies in excess of 25% to be realised over a wide range of 'duty factor'.

8 Acknowledgments

The authors would like to thank S.M.R. Gordon for the fabrication of the trapatt diodes. Thanks should also be given to A.L. Eldridge, P.R. Wickens and M.R. Weatherhead for their previous contributions.

The authors are indebted to I.W. Mackintosh and R.J. Royds of the RSRE, Malvern, England, for many useful and encouraging discussions throughout the development of these devices.

This work has been carried out with the support of the Procurement Executive of the UK Ministry of Defence; it is sponsored by DCVD and is published with the permission of the Directors of the Plessey Company Limited.

9 References

1 PRAGER, H.J., CHANG, K.K.N., and WEISBROD, S.: 'High power, high efficiency silicon avalanche diodes at ultra frequencies', *Proc. IEEE*, 1967, 55, pp. 586–587

2 PURCELL, J.J., WEATHERHEAD, M.R., GORDON, S.M.R., OXLEY, C.H., and WICKENS, P.R.: 'High-efficiency TRAPATT operation in X-band', *Electron. Lett.* 1975, 11, pp. 236–238

3 FONG, T.T., and YING, R.S.: 'Complementary X-band TRAPATT diodes', IEEE International Microwave Symposium, Atlanta, G., USA, June, 1974

4 BAXANDELL, P.J., COLLIVER, D.J., and FRAY, A.F.: 'An instrument for the rapid determination of semiconductor impurity profiles', *J. Phys. E.*, 1971, 4, pp. 221–213

5 BICKNELL, R.W.: 'A simple rotating jet-thinning apparatus for producing taper sections and electron microscope specimens from silicon and compound semiconductors', *J. Phys. D.*, 1973, 6, pp. 1991–1997

6 CURTICE, W.R., RISKO, J.J., and HO, P.T.: 'A study of second-harmonic-extraction TRAPATT amplifiers for X-band operation', *RCA Rev.*, 1975, 36, 274–295

7 EVANS, W.J.: 'Circuits for high-efficiency avalanche diode oscillators', *IEEE Trans.*, 1969, MTT-17, pp. 1060–1067

8 TREW, R.J., HADDAD, G.I., and MASNARI, N.A.: 'The operation of S-band TRAPATT oscillators with tuning at multiple harmonic frequencies', *Ibid.*, 1975, MTT-23, pp. 1043–1047

9 TREW, R.J., MASNARI, N.A., and HADDAD, G.I.: 'Circuit optimization of S-band TRAPATT oscillators', IEEE International Symposium, Georgia Institute of Technology, Atlanta, G., USA, 1972

10 SLAYMAKER, N.A., CARROLL, J.E., and DEBOISE, R.H.: 'Efficient power extraction at TRAPATT harmonics', *Electron. Lett.*, 1970 6, pp. 744–746

11 CRIPPS, S.C., and CARROLL, J.E.: 'Double-diode TRAPATT pulse generator with applications to avalanche-diode research', *Proc IEE*, 1975, 122, (11), pp. 1187–1192

12 ROSEN, A., REYNOLDS, J.E., LIU, S.L., and THERIAULT, G.E.: 'Wideband class-C TRAPATT amplifiers', *RCA Rev.*, 1972, 33, pp. 729–736

13 CARSLAW, H.S., and JAEGER, J.C.: 'Conduction of heat in solids', (Clarendon Press, Oxford, 1958)

SUBMISSION OF NEW INVENTION — PATENT FORM A

This form should be completed, signed by inventor(s) and your departmental head and submitted with an attached description of the invention to your GROUP PATENT REPRESENTATIVE for transmission to Patent Department, Ilford.

From: Allen Clark Research Centre, Caswell, (Div./Location/Group) Towcester, Northants. Optoelectronics & Microwave Dept. Date: 16.12.76.

Quoting Reference (e.g. Dept. No.) 202

1. Title of Invention:

RUGGED COAXIAL MICROWAVE CAVITY

2. Brief description of nature and objects of invention: A microwave coaxial
ity constructed by reproducing the matching conditions presented by the movcable slugs of
vontional circuits, by means of metal plates, have appropriately sized irises. The plates
clampod together, enabling the characteristics of the conventional slug-tuned circuit to be
oduced in a form capable of withstanding severe shock and vibration.

ctive
abricate a coaxial micro-
system capable of with-
ding severe environmental
tions.

A full description (with drawings where appropriate in duplicate) should be attached to this form, with answers, if possible, to the following questions:-

(a) What were you aiming to achieve? (b) In what way is your proposal an improvement on present ways of obtaining the same result? (c) Are there any other new ways likely to become useful as a means of avoiding any patent obtained for your present proposal? What difficulties would avoidance entail? (d) What is the immediate application and what other uses do you visualise, not necessarily in your own field of activity? (e) What are the inventive features and how would you define them in your patent claim(s).

3. Product, system, etc. in connection with which invention was devised:

X-band TRAPATT Coaxial Amplifier Circuit

4. Has the invention been tried out in practice ?
Yes

5. Anticipated date of first commercial use of invention, or of publication or disclosure other than within Plessey : February 1977

6. At the time the invention was made were the inventors working at Government expense? If so, give contract number including number of relevant patent clause, and name of Ministry responsible.

Yes. Ministry of Defence (VX9399)

7. Indicate security classification of invention, if any: None

8. Has the invention any connection with any licence or other agreement? Please give details.
No

9. Was any part of the invention derived from an outside source ?
No

10. Full Christian name, surname, home address and nationality of each person claiming to be an inventor:-

Christopher Hunter Oxley. British
Allen Clark Research Centre,
Caswell, Towcester, Northants.

Signed: C.H. Oxley — Inventor(s)

Approved: J.T. Pratt

Suggested Sponsor:

FOR PATENT DEPARTMENT USE

Date received:

Assigned to:

Subject Classification:

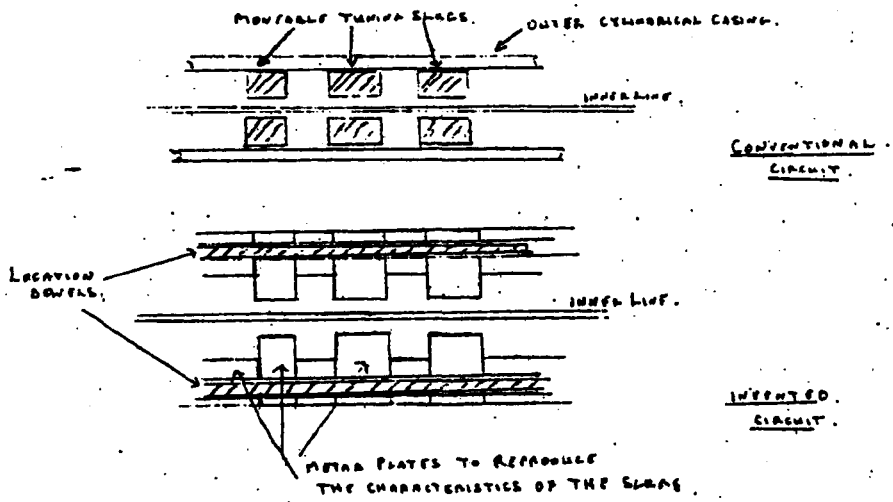
Case No:

169

CIRCUIT DESCRIPTION

A conventional coaxial microwave circuit comprises an outer cylindrical casing, an inner line and a number of moveable tuning slugs supported by either the inner or outer-line surfaces. The slugs effect distributed impedance perturbations, enabling complex impedance transformations to be realised. Coaxial circuits are widely used as filters, impedance transformers and resonant cavities; however their mechanical fragility frequently precludes their use in hostile environments.

The invented circuit consists of a number of metal plates of various thicknesses, having holes formed along a common axis. Three plates are mounted together to reproduce the characteristics of the slugs in the conventional circuit. Shims may be used to adjust the relative position of the sections, so providing a means of fine matching. Dielectric or metallic screws may also be inserted through the metal sections, to protrude into the air-line, providing an extra degree of fine tuning. The microwave performance of this circuit has been found to be similar to that of the existing circuit. The plates can be located by means of dowels and may be clamped firmly together, enabling an adjustable coaxial circuit to be realised in a rugged form appropriate for commercial and military use.



130

Locked oscillator power combining through a Wilkinson coupler

M.W. Geen, B.Sc. (Eng.), T.J. Brazil, B.Eng., Ph.D., Mem. I.E.E.E., and C.H. Oxley, B.Sc., C.Eng., M.I.E.E.

Indexing terms: *Oscillators, Semiconductor devices and materials, Electromagnetics, Waves and wave scattering*

Abstract: The paper describes the combining of power for *J*-band pulsed InP locked oscillators via a Wilkinson coupler. A simple theoretical model for a pulsed locked oscillator is presented. The model is then used to demonstrate the power combination of two pulsed locked oscillators via a Wilkinson coupler. The resulting bandwidth and combining efficiency are very sensitive to the *Q*-chirp products, values of external *Q* and relative output amplitudes of the oscillators. The theoretical results are compared with experimental data, and it is concluded that this technique of power-combining pulsed *J*-band sources will only give a useful operational bandwidth of 1–2%.

1 Introduction

Solid-state devices can offer a number of advantages when compared to sources made by using vacuum devices. One particular advantage is lower operating voltage, when compared with the 'tube sources', and, therefore, the elimination of high-voltage multipliers. The solid-state source can also offer medium peak-power levels (10–50 W) with considerable frequency agility. At present the high-efficiency pulsed TWT is still in development; whereas the magnetron, although offering the peak power and efficiency, will only operate over relatively narrow bandwidths.

A number of techniques are available for increasing the peak power of a solid-state transmitter, these are:

(*a*) manufacturing a larger area device

(*b*) chip combining at package level

(*c*) circuit combining, by power addition from a number of separate devices or resonant cavities.

The first of these methods will ultimately not only present a diode reactive component which is too large to match in a circuit (the PZF[2] limitation), but also the skin effects within the device can become comparable with the negative resistance of the device at high frequencies, and so making the diode very inefficient. The second technique suffers from package and bond-lead parasitics, which can limit operating frequency, reduce power-combining efficiency and lead to poor reproducibility. The third technique is power combining at the circuit level, which allows power addition from existing diode and packaging techniques.

The method reported here was to use a 3 dB Wilkinson combiner and separate resonant cavities; a technique which has been successfully employed at lower frequencies [1] and offers the advantages of using sensible area diodes with well characterised packages and cavities.

The paper describes the experimental use of the coupler in combining pulsed sources, and the theoretical limitations of using this method at high frequencies for pulsed sources over wide bandwidths.

2 Coupler description

The basic Wilkinson coupler is of the form shown in Fig. 1; for convenience port 1 will be referred to as the output, and ports 2 and 3 as the inputs.

Ideally, the resistor should have linear dimensions which are negligible, compared to a wavelength at the centre frequency, and be nonreactive. These requirements are necessary to maintain the correct phase relationships to give isolation between the input ports [2]. Additionally, there should be no coupling between the $\lambda/4$ lines as this will reduce the isolation between ports 2 and 3; this requirement implies widely spaced $\lambda/4$ lines. As the operating frequency is increased it becomes more difficult to meet these requirements and careful attention must be paid to the geometry of the coupler.

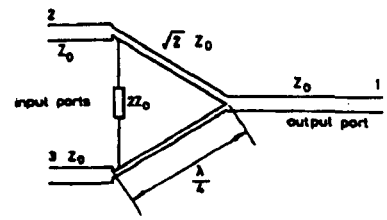


Fig. 1 *Wilkinson coupler*

A computer program to analyse the Wilkinson coupler assuming TEM propagation was developed by T.J. Brazil. The quasi-TEM mode, as propagated on microstrip, is described by including the effective dielectric constant of the medium. The program cascades the scattering matrices of the Wilkinson coupler with the scattering matrices which describe lengths of transmission line, lumped capacitors and resistors; thereby allowing the inclusion of simple parasitic junction effects [3]. In this way it is possible to analyse, to a first approximation, practical geometrical coupler structures and so reduce the amount of initial experimental work. The computer program was used to calculate VSWR, isolation and insertion loss for each port of the coupler; assuming that the other ports are terminated with 50 Ω loads.

The use of the analysis computer program, in conjunction with experimental coupler work, lead to the Wilkinson coupler design, shown in Fig. 2*a*. This coupler design was used for all the experimental work described in this paper.

The technological problems in producing the coupler were numerous; because at these frequencies (16–18 GHz) *Y*-junction parasitics, isolator resistor parasitics and substrate mounting techniques all play a major part in the overall RF performance of the coupler.

The couplers were fabricated using both thin and thick film fabrication techniques, and the experimental results demonstrate only a marginal difference of insertion loss and isolation between the couplers, made by using both manufacturing methods. Indeed the similarity in RF performance

Paper 1804H, received 17th August 1981

Mr. Geen and Mr. Oxley are, and Dr. Brazil was formerly, with the Allen Clark Research Centre, Plessey Research Limited, Caswell, Towcester, Northants. NN12 8EQ, England. Dr. Brazil is now with the Department of Electrical & Electronic Engineering, University College, Upper Merrion Street, Dublin 2, Eire

0143–7097/82/020077 + 06 $01.50/0

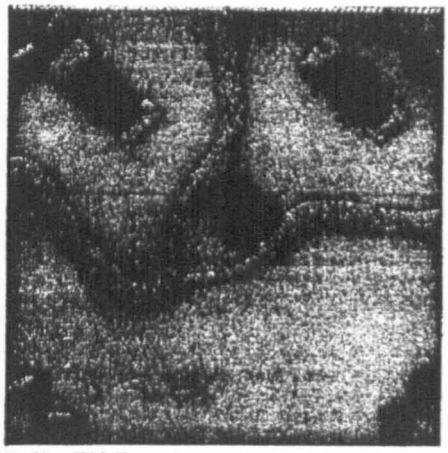


Fig. 2A *Thick-film coupler with test resistors*

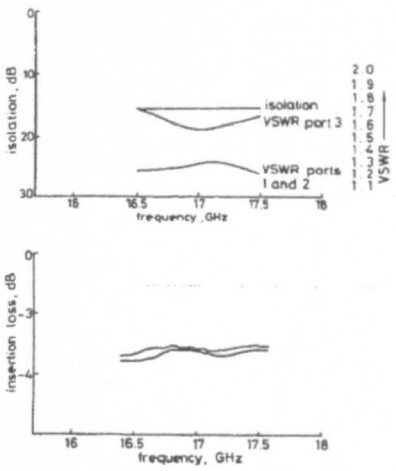


Fig. 2B *Experimental RF performance of Wilkinson coupler*

of both couplers demonstrates the feasibility of using thick-film technology for circuits operated at upper *J*-band frequencies. In large-quantity production, thick-film technology may offer a much cheaper manufacturing solution than thin-film techniques. Fig. 2*b* shows the typical measured performance of the thick-film coupler.

3 Power combining

The active devices used in the power-combining experiments were pulsed indium phosphide [6] (InP) transferred-electron diodes, with gold integral heat sinks (IHS). These devices offer greater efficiency and with similar peak powers to GaAs TE diodes. At upper *J*-band frequencies, efficiencies of 18% and peak powers of 15 W have been experimentally observed [7]. The '*Q*-chirp' product is a figure which was found convenient in the description of a pulsed diode in a resonant cavity. This number describes the product of the external Q of the oscillator and the mean-frequency chirp rate within the RF pulse width. The Q-chirp product for a typical 200 μm diameter InP IHS is 4000 MHz/μs (for a 1 μs pulse width and an external Q of 10, the frequency chirp of the diode is approximately 400 MHz).

Using a more generalised form of Alder's equation [8–11]

$$Q_e = \frac{2W_0}{\Delta W}\left(\frac{P_{in}}{P_0 - P_{in}}\right)^{1/2}$$

where P_{in} is the locking power and P_0 is the output power and ΔW is the total frequency deviation, it can be shown that to obtain approximately 1 GHz operational bandwidth, with a gain of 10 dB, the external Q of the cavities should be of the order of 10. Coaxial cavities were used because an external Q of this order could be obtained; microstrip was not considered because of the difficulties experienced in matching large-area low-impedance diodes into this transmission medium.

Experiments were carried out to investigate power combination using two nominally identically coaxial cavities

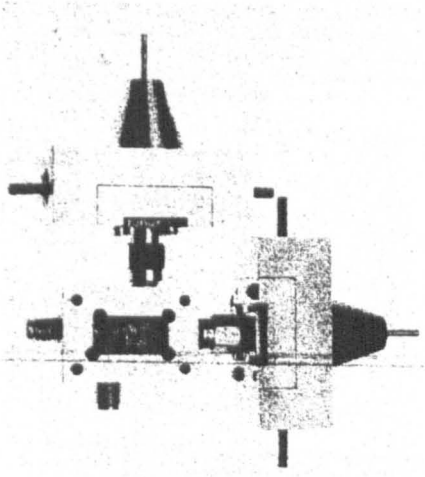


Fig. 3 *Assembly of two coaxial cavities and Wilkinson coupler*

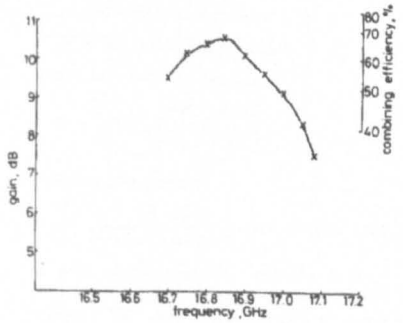


Fig. 4 *Experimental locking bandwidth of two cavities combined via a Wilkinson coupler*

combined using the Wilkinson coupler (Fig. 3) and injection locked to a PIN modulated TWT source. The locking gain was typically 10 dB. The apparent practical advantage of this form of power combining was that each cavity could be separately set up and tested, before being assembled to the previously characterised coupler. The experimental results (Fig. 4) show that the expected locking bandwidth was not obtained and the combining efficiency was degraded, particularly near the edge of the locking band. This limits the useful operational bandwidth which may be obtained with this method. The maximum combining efficiency which could be obtained was approximately 90% (excluding the base loss in the coupler); but only over a relative narrow band, approximately 100 MHz.

The perfomance of the Wilkinson coupler is sensitive to the phase and amplitude inbalance at the input ports; hence, to obtain maximum power combination, both oscillators should track with equal phase and amplitude across the required bandwidth. Fig. 5 is an experimental plot of insertion loss against phase difference between two RF signals applied to the input ports of the coupler.

3.1 *Theoretical model for pulse power combining through a Wilkinson coupler*

A pulsed locked oscillator exhibits both an impulse phase characteristic and a phase locking characteristic. The former is attributed to the impulse temperature sensitivity of the device impedance, and the latter to the change in cavity impedance from the value at the free-running frequency of the oscillator; both contribute to the overall phase of the oscillator and are interrelated. The work summarised in this paper extends the CW locked oscillator model of Quine [10] to include a frequency chirp term which would be found in a pulsed locked oscillator. The results from the model are then used to demonstrate how sensitive this form of power combining is to the external Q, Q-chirp product and relative amplitude of the sources.

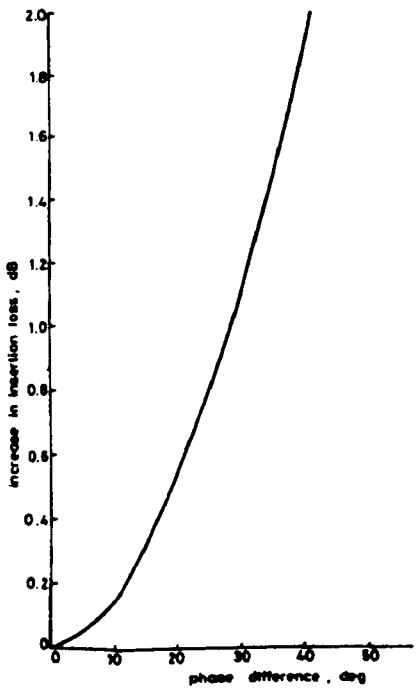


Fig. 5 *Phase difference against insertion loss*

3.2 *Pulsed locked oscillator*

Quine [12] has combined a simple negative-resistance oscillator, with the locking signal injected via an ideal lossless circulator, providing a perfect match (Fig. 6). To satisfy the normal transmission-line equations, Quine shows that the input admittance Y_{IN} at the diode side of the transformer is given by

$$Y_{IN} = \frac{Y_0(1 - V_1^2)}{n^2(1 + 2V_1\cos\theta + V_1^2)} + j\frac{Y_0 2V_1 \sin\theta}{n^2(1 + 2V_1\cos\theta + V_1^2)} \quad (1)$$

where $V_1^{-1} = a_i/b_r$ and is the normalised voltage gain of the locked oscillator, a_i is the incident voltage and b_r the resulting voltage, respectively, at the input and output ports of the ideal circulator and Y_0 is the characteristic admittance of the output transmission line.

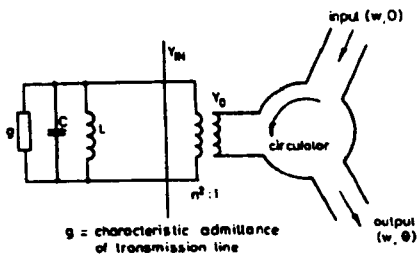


Fig. 6 *Circuit diagram of locked-oscillator model*

At the locking frequency W the oscillator susceptance is B, and w_0 is the free-running frequency of the oscillator; we then have the following for B:

$$B = WC - \frac{1}{WL} = W_0 C\left[\frac{W}{W_0} - \frac{W_0}{W}\right] \quad (2)$$

If the oscillator has chirp then:

$$W = W_0 + \Delta W_c\,(\text{chirp}) + \Delta W$$

where $\Delta W_c + \Delta W \ll W_0$. Hence

$$B = 2W_0 C\left[\frac{\Delta W}{W_0} + \frac{\Delta W_c}{W_0}\right]$$

Equating susceptances:

$$\frac{Y_0}{n^2}\left[\frac{2V_1 \sin\theta}{1 + 2V_1\cos\theta + V_1^2}\right] = 2C(\Delta W + \Delta W_c) \quad (3)$$

to obtain an expression for the frequency chirp it was assumed that the oscillator susceptance changes with time and frequency.† This model has been used to satisfactorily explain the amplitude and frequency behaviour of cavity-stabilised pulsed oscillators.

For convenience we assume at a frequency w_0 and time

$t = 0$, the total oscillator susceptance is zero, and the load conductance $g_L = 1$:

$$\bar{B}(W_0, t) = \frac{-2g_L Q_e(W_0 - W)}{W_0} - \alpha t$$

where α is the rate of change of device susceptance. The following condition must be satisfied, for all t:

$$\bar{B}_{device} + \bar{B}_{circuit} = 0$$

Therefore

$$\Delta W_e \text{ (chirp)} = \frac{-W_0 \alpha t}{2Q_e} \quad (4)$$

Substituting $Q_{ext} = \pi^2 C W_0 / Y_0$ (from WL/R formula), and eqn. 4 into eqn. 3, gives:

$$\frac{2V_1 \sin\theta}{1 + 2V_1 \cos\theta + V_1^2} = \frac{2Q_e \Delta W}{W_0} - \alpha t$$

Now let $C_1 = k - \alpha t$ where C_1 is time dependent and $k = \frac{2Q_e \Delta W}{W_0}$, the following transcendental equation is obtained:

$$\frac{2V_1 \sin\theta}{1 + 2V_1 \cos\theta + V_1^2} = C_1$$

The solution for θ, the phase of the locked oscillator relative to the input locking signal, is given below [13]:

$$\theta = \sin^{-1}\left\{\frac{C_1}{\sqrt{1 + C_1^2}}\left[\frac{1 + V_1^2}{2V_1}\right]\right\} + \sin^{-1}\left[\frac{C_1}{\sqrt{1 + C_1^2}}\right] \quad (5)$$

θ also time dependent through the term C_1.

Therefore the phase and amplitude solution for each locked oscillator, at a given pulse width, may be described as follows:

$$OSC_1(f) = F(V_{11}, \theta_1)$$
$$OSC_2(f) = F(V_{12}, \theta_2)$$

The model can be extended to consider locking two oscillators from a common locking source, and then combining the outputs via a Wilkinson coupler. The circuit is shown in Fig. 7.

To make use of the simple pulsed locked oscillator model already described, it was assumed that both oscillators were matched to an ideal lossless circulator; the outputs from each oscillator $F(b_{r1}, \theta_1)$ and $F(b_{r2}, \theta_2)$ were then combined via a Wilkinson coupler. In assuming that the circulators are ideal and lossless, they may be excluded and the model approaches the more usual configuration when using a Wilkinson coupler as a power-combining element (Fig. 8).

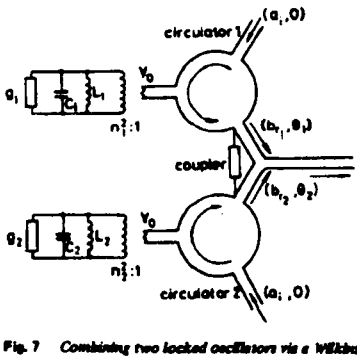


Fig. 7 *Combining two locked oscillators via a Wilkinson coupler*

To allow for a more realistic description of the oscillators, the normalised voltage gains of each oscillator when locked were described as functions of frequency ($V_1 = F_1(f)$). These expressions can be deduced for the experimental locked oscillators by fitting polynomials of order n to the experimental gain-frequency plots and then deriving the normalised-voltage/gain-frequency curves for the oscillators.

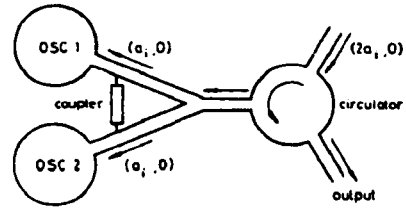


Fig. 8 *Usual circuit configuration for power combining via a Wilkinson coupler*

The Wilkinson coupler was simulated by using two polynomials. The polynomials describe the increase in insertion loss of the coupler with phase and amplitude imbalances, respectively, at the input ports of the coupler.

The polynomials were derived from curve-fitting methods to experimental results of a measured coupler. This method was chosen as it realistically characterised the nonideal behaviour of the coupler described in this work.

The differences in phase $|\theta_1 - \theta_2|$ and amplitude $|b_{r1} - b_{r2}|$ between the oscillators may be computed over a specified bandwidth. These values may then be substituted into the polynomials describing the coupler and the computed increased insertion loss of the coupler. The value may then be added to the base-line insertion loss of the coupler owing to radiation, conduction and dielectric loss factors of the microstrip configuration and material; this value was taken to be 0.5 ± 0.1 dB. The combining efficiency may then be computed over the specified bandwidth.

With these points in mind, it is possible to predict the performance of two locked pulsed oscillators combined using a Wilkinson coupler. The two locked oscillators were assumed to have an external Q of 10, a gain of 10 dB and a Q-chirp product of 4000 MHz/μs. Each of the three parameters of one oscillator was changed in turn, and the effect upon the combining efficiency of the whole unit over a required bandwidth was computed.

Fig. 9 shows the computed effect of changing the Q-chirp product of one of the oscillators from 2000 to 9000 MHz/μs. The parameter not only changes the centre frequency of the unit, but can have a large effect upon the combining efficiency of the unit. The Q-chirp product is diode dependent and, therefore, the overall combining efficiency of the unit will be subject to the repeatability of this parameter from diode to diode. Within a batch of 200 μm-diameter indium-phosphide IHS diodes, operated in a test circuit, the Q-chirp product can vary between 1500 and 4500 MHz/μs.

Fig. 10 shows the effect upon the combining efficiency, as the external Q of one of the cavities is changed from 10 to 60. The overall effect is a reduction of the usable bandwidth of the unit. Small external Q-values are difficult to measure by either common technique of load pulling or injection locking, and it is possible to incur large errors up to $\pm 50\%$. Consequently, difficulties would be encountered in setting up

† From a private communication by M. Brooksbanks, to be published

two separate oscillators of identical external Q, of the order of 10, to fulfil the required 5% bandwidth at upper J-band frequencies.

The effect of a gain difference between two oscillators is shown in Fig. 11. Although a gain difference of 1 dB will have little effect on the combining efficiency at the centre frequency, it will have a much greater effect at the band edges. In practice, it is possible to achieve closely matched gains (at least at centre frequency) by well controlled setting-up procedures.

4 Comparisons with experimental results

Two low-Q coaxial cavities were set up, using 200 μm-diameter IHS indium-phosphide diodes. The gain-frequency characteristics of each oscillator were measured and fully described by two second-order polynomials. The microstrip coupler was described by two polynomials. Fig. 12 compares the experimental and theoretical results. For the theoretical model it was assumed that the two diodes had different Q-chirp products of 4000 and 2000 MHz/μs, which are within the measured range for this type of diode. The external Q-values were taken to be 10 and 20, which were within the error limits of the experimentally measured values. From many experimental observations of TE devices operating in resonant structures with Q_e-values, in the range 50 to 500, the chirp (ΔF) and the Q_e are related by the expression $\Delta F \propto (Q_e)^p$, with $-1.225 < p < -1.24$; consequently the

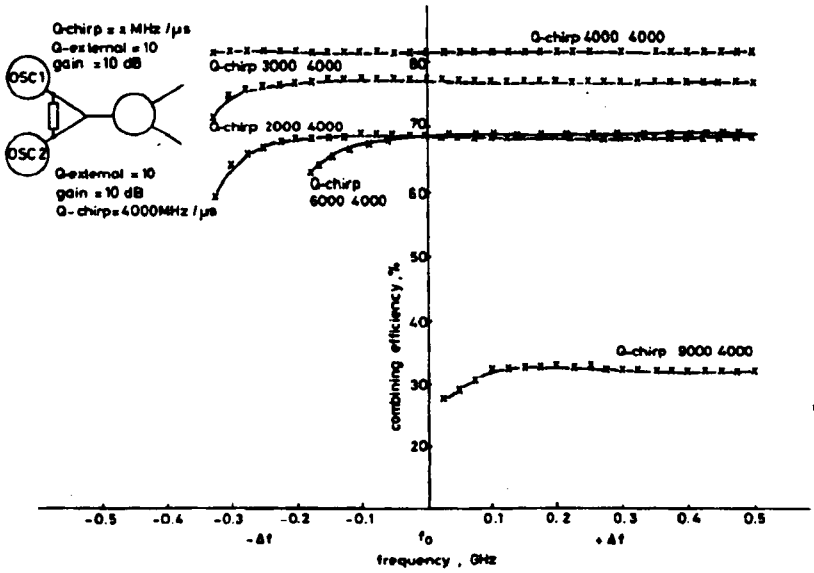


Fig. 9 *The effect on combining efficiency in changing the Q-chirp product of one of the oscillators*

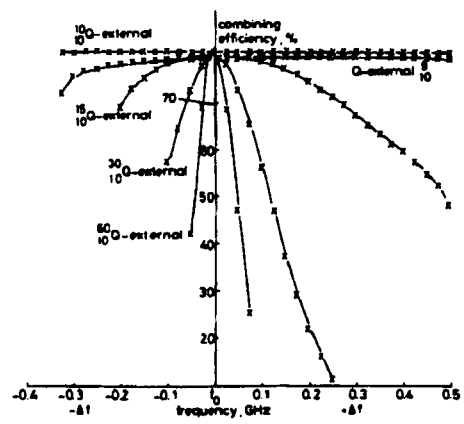


Fig. 10 *The effect on the combining efficiency if Q_e of one of the oscillators is changed*

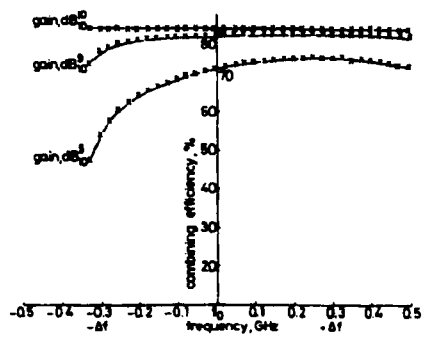


Fig. 11 *The effect of the combining efficiency if the gain of one of the oscillators is changed*

Q-chirp product is related to the external Q by the expression $(\Delta F\, Q_e) \propto Q_e^{p+1}$, with $-0.22 < p + 1 < -0.24$.

The curve (Fig. 12) represents the typical bandwidth which could be reasonably obtained from this form of power combining structure.

5 Conclusions

The advantage of power combining two oscillators, using a Wilkinson coupler, is that the Wilkinson coupler and each oscillator can be individually set up and tested. This method also allows higher power to be obtained, without having to develop a larger diode or new resonant cavities. Although this technique appears to be successful at lower frequencies

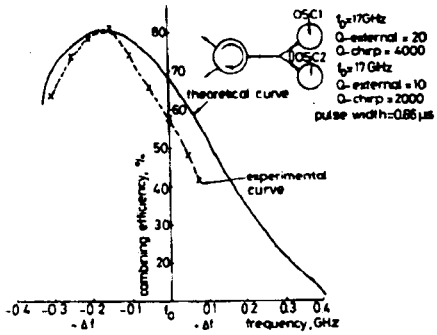


Fig. 12 *Comparison between theoretical and experimental data for power combining two pulsed InP oscillators through a Wilkinson coupler*

and for CW sources, a number of disadvantages have been encountered when considering high-frequency and pulse-modulated oscillators.

The analysis and experimental results show a severe limitation in efficient power combining over a wide bandwidth, especially for pulsed oscillators. The Q-chirp product of the pulsed indium-phsophide oscillators is not exactly reproducible and this parameter has a large influence on the resulting power-combining efficiency. In addition, for only a 5% bandwidth in upper J-band, at 10 dB gain, an external Q of 10 is required. Low values of Q_e are notoriously difficult to measure, particularly for pulsed oscillators with chirp, and the analysis has highlighted the dependence of bandwidth on the external Q to each cavity being matched within ± 10%. This parameter applies not only to pulsed oscillators, but also to CW oscillators. To conclude, in J-band, using this technique of power combining pulsed sources with a significant Q-chirp product and accepting only a 1 dB variation in output power, then a realistic bandwidth would only be 1–2%. This bandwidth would be greater if the method were used in combining CW sources.

Extending this technique to a Wilkinson tree network, as referenced by Russel [14] at J-band frequencies using pulsed sources, would be impractical for a broadband transmitter.

6 Acknowledgments

The authors would like to thank Mr. M. Hepher and Mrs. O. Townsend for thick-film fabrication, Mr. J. Sparrow and Dr. C. Suckling for thin-film fabrication, and Dr. R.L. Tebbenham for useful discussion.

This work has been carried out with the support of the Procurement Executive, Ministry of Defence, sponsored by DCVD.

7 References

1 FUKUI, H.: 'Frequency locking and modulation of microwave silicon avalanche diode oscillators', *Proc IEEE*, 1966, 54, pp. 1475–1477

2 WILKINSON, E.J.: 'An N-way hybrid power divider', *IRE Trans.*, 1960, MTT-8, pp. 116–118

3 GUPTA, C., and GOPINATH, A.: 'Equivalent circuit capacitance of microstrip step change in width', *IEEE Trans.*, 1977, 10, pp. 819–822

4 COHN, S.B.: 'A class of broadband three-port TEM mode hybrids', *ibid.*, 1968, MTT-16, pp. 110–116

5 PARAD, L.I., and MOYNIHAN, R.L., 'Split-tee power divider', *ibid.*, 1965, MTT-13, pp. 91–95

6 IRVING, L.D., PATTISON, J.E., BRADDOCK, P.W., and GRAY, K.W.: 'Improved mean power and long pulse-width operation of InP t.e.o.s in J-band', 1978, *Electron. Lett.*, 14, (4), pp. 116–117

7 BRAMBLEY, D.R., and SMITH, D.C.: 'High-efficiency InP transferred electron device for high peak power, high mean power pulsed sources in J-band', *ibid.*, 1981, 17, (8), pp. 307–308

8 ADLER, R.: 'A study of locking phenomena in oscillators', *Proc. Inst. Radio Engrs.*, 1946, 34, pp. 351–357

9 HOBSON, G.S.: 'Measurement of external Q-factor of microwave oscillators using frequency pulling or frequency locking', *Electron. Lett.*, 1973, 9, (10), pp. 191–193

10 DIAMOND, F.G. and ARMAND, 'External Q-factor measurements of an oscillator by the injection locking ellipse', *ibid.*, 1972, 8, (16), pp. 406–407

11 HINES, M.E.: 'Negative-resistance diode power amplification', *IEEE Trans.*, 1970, ED-17, pp. 1–8

12 QUINE, J.P., 'Injection phase-locking characteristics of LSA-mode Transferred electron oscillators', *Proc. IEEE*, 1969, 57, pp. 715–717

13 MICHAELIDES, M., and STEPHENSON, I.M.: 'Injection locking of microwave solid-state oscillators', *ibid.*, 1971, 59, pp. 319–321

14 RUSSELL, K.J.: 'Microwave power combining techniques', *IEEE Trans.*, 1979, MTT-27, pp. 472–478

APPENDIX 6 (continued)

Reference to these published works in the text are denoted by the letter B, for example [B1]

1) C.H.Oxley 'Active devices suitable for millimetric wave operation' Colloqium on millimetre operation, IEE, Digest 1986/109, November 1986.
2) *C.H.Oxley and A.J.Holden 'Simple models for high-frequency MESFETs and comparison with experimental results' IEE Proc, Vol.133, Pt. H, Nos 5, Oct 1986.
3) *C.H.Oxley and A.J.Holden 'Modified Fukui model for high frequency MESFETs' Elec. Lett, 22, 1986, 690-692.
4) C.H.Oxley 'In two decades to millimetric wave gallium arsenide FETs', Allen Clark Research Centre Annual Review, 1985, pp 97-104.
5) *C.H.Oxley 'Q-Band (26-40GH_z) 'GaAs FET Single-Stage Amplifier', Electronics Letters, 18th March 1982, Vol.18, Nos 6.
6) C.H.Oxley, J.Arnold and J.Sparrow 'Q-BAND Microstrip Techniques' IEE Colloquium, April 1982.
7) *C.H.Oxley, A.H.Peake, R.H.Bennett, J.Arnold and R.S.Butlin 'Q-BAND (26-40 GH_z) GaAs FETS, Proc IEDM, Washington, 1981.

Non first authored papers containing further research work carried out by the author:

8) *A.J.Holden, B.T.Debney, J.P.King, J.G.Metcalfe and C.H.Oxley 'Matching of GaAs power FETs using a large signal modelling technique' IEE, Proc Pt. H. 133, 1986, pp399-403. (Hard copy not included)
9) *A.J.Holden, I.Davies, P.Medhurst, and C.H.Oxley 'New wideband GaAs travelling wave device: linear gate transistor' Elec.Lett. 22, 1986, pp 777-778.
10) I.Davies, D.Brambley, R.Bennett, A.Powell, and C.H.Oxley 'The design and performance in Q-band of 0.3 micron gate-length MESFETs, ESSDERC' 85, Aachen, Germany, 9-12th September 1985. (Hard copy not included).
11) M.D.Scott, A.H.Moore, I.Griffith, R.J.M.Griffiths, R.S.Sussmann, C.H.Oxley 'MOCVD Growth of AlInAs/GaInAs MESFET Heterostructures' ESSDERC' 85, Aachen, Germany, 9-12th September 1985. (Hard copy not included).
12) *A.J.Holden, D.R.Daniel, I.Davies, C.H.Oxley and H.D.Rees 'Gallium arsenide travelling wave field-effect transistors' IEEE, ED-32, pp 61-66, 1985.

ACTIVE DEVICES SUITABLE FOR MILLIMETRE WAVE OPERATION

C.H.OXLEY (Plessey Microwave)

Over the recent years there has been an upsurge of interest in milli-metric wave applications (secure communications, radiometry, high resolution radars, intelligent munitions etc) and with the development of improved material and technologies has lead to an increase in the development of milli-metric wave active devices. In particular the work has seen the transistor being developed with an Fmax well in excess of 100GHz, (1) and very recent work from the USA has report the first transistor amplifier measurements around 94GHz (2). The work has also seen the continued development of the two terminal transfer electron device (TED), IMPATT and multiplier diodes.

This paper will discuss some of the possible three terminal device structures (MESFETS, HEMT, BHJT, CHINT, VMT) suitable for milli-metric wave operation, along with predicted and experimental rf performances. The geometry of most of the transistor types will enable the development and fabrication of milli-metric microwave monolithic integrated circuits (MMMIC) and this is possibly the greatest driving force for this component. To obtain high-frequency performance the transistor geometry has to be shrunk in order to minimise the input capacitance, but unfortunately his may severely limit the output power from these structures to around the 10mW (cw) level. Therefore to obtain a high output power two terminal devices will need to be considered. Work on these devices has continued and with careful design, in particular the thermal characteristics, cw output powers exceeding of 250mW at 100GHz have been recorded using silicon IMPATT diodes. The integration of both Gallium Arsenide transistor and silicon two terminal device technologies may be feasible with the recent development of gallium arsenide (GaAs) grown on silicon.

To obtain operation from any device at milli-metric wave frequencies, the associated device parasitics need to be minimised. In particular for both the HEMT and MESFET the gate-length is reduced to raise the frequency of operation of the transistor. Technologically the gate length can be reduced to well below 0.1 microns, using electron beam lithography (3). In practise the reduction in the gate length may be limited by the geometrical parasitics eventually dominating the structures. Also at very high frequencies the device geometry may become comparable to a wavelength and therefore the transistor will have to be considered as a distributed network. Recent work at Plessey has indicated that distributed effects may give rise to deviation from the Fukui noise theory. Work will be presented giving a simple empirically derived modified version of the Fukui noise theory (4), which may be used to describe the noise figure of both MESFETs and HEMT devices out to milli-metric wave frequencies. A comparison between the simple modified Fukui noise theory and experimentally measured noise figures to 60GHz are given in Table (1) :

Table 1

Device Type	Frequency	Measured Noise Figure	Predicted Noise Figure
	GHz	dB	dB
Plessey high-frequency FET (Variant 1)	32	3.7	3.8
NEC 673	22	2.6	2.6
Hughes	30	2.0	2.1
Plessey high-frequency FET (Variant 2)			
Hughes	60	>5.0	5.75

The Plessey device variants are similar to the transistor which was used in the development of a Q-band amplifier (5). The present work indicates that the HEMT transistor will give the lowest noise figure at high frequencies, and as it is a relatively new structure its reliability still needs to be proven.

The output power of a milli-metric HEMT device may be increased, when compared with a MESFET, by using multiple quantum wells (6). Although at present it is still difficult to see a transistor capable of producing an output power comparable to a silicon IMPATT diode at milli-metric wave frequencies (40-140GHz).

In the milli-metric wave region there are two solid state devices which are presently available as power sources, these are the IMPATT and transfer electron device. Undoubtedly the silicon IMPATT diode offers the highest output power (1 watt CW, and >15 watts pulsed at 94GHz), while the TED device will offer a lower output power with good close to carrier noise characteristics. The design and technology aspects for both device types along with the mode of operation will be briefly described. One of the major problems is to minimise the operating junction temperature, by improving the thermal design of the diodes by utilising gold and diamond heatsink technologies. Obviously, the device and circuit parasitics need to be minimised, and recent work has been published (7) in which GaAs IMPATTS and matching circuits have been fabricated as an integrated circuit.

A comparison between the RF performance of Plessey GaAs TED and silicon IMPATT diodes to frequencies approaching 100GHz will be presented, along with the noise performance characteristics. Published work by Eddison (8) has indicated that a comparable noise performance (1KHz from carrier) may be operated for both GaAs, InP TEDs and silicon IMPATT diodes provided the latter are operated at a reduced bias level. In recent years great advances have been made in milli-metric wave transistors, but it is difficult to see a 3 terminal device on the horizon which will give an output power comparable to existing IMPATT and TED devices. Work on two terminal devices is progressing into developing a technology which is compatible with GaAs MMICs and predictions are being made (9) concerning the fabrication of a new generation of two terminal devices using differential mobility within super-lattice structures to further enhance RF performance (output power, efficiency etc.) at milli-metric wave frequencies.

Acknowledgements

Part of this work was carried out with the support of the procurement executive, Ministry of Defence (Directorate of Components Valves and Devices) sponsored in part by the Royal Signals and Radar Establishment.

The Author is indebted to his colleagues at Plessey Research Caswell Ltd for their contributions to this paper.

References

1. H.Tserng and B.Kim 'A 115GHz monolithic GaAs FET oscillator' 1985 GaAs IC Symposium

2. P.M.Smith, P.C.Chao, K.H.G. Duh, L.F.Loster and B.R.Lee '94GHz transistor amplification using a HEMT Electronic Letters' July 1986

3. W.Patrick, W.S.Makie, S.P.Beaumont, C.D.W.Wilkinson and C.H.Oxley 'Very short narrow gate-length GaAs MESFETs' Electron Device Letters, September 1985.

4. C.H.Oxley and A.J.Holden, 'Modified Fukui Model for high-frequency MESFETs' Electronic Letters, June 1986

5. B.Clark, D.Watkins and B.Mazonas 'K Band FET Amplifier' IEE Colloquium November 86 on 'Millimetre wave component design' 1986.

6. A.K.Gupta, R.T.Chen, E.A.Sovero and JH.A.Higgins 'Power Saturation characteristics of GaAs/Al GaAs High mobility transistors' Monolithic circuits symposium, 1985.

7. B.Bayraktaroglu and D.Shi 'High power 60GHz monolithic GaAs Impatt Diodes' Electronics Letters, May 1986.

8. I.Eddison 'Noise in millimetre wave oscillators' Journal IERE, May 1985.

9. R.Grondin and J.Wang 'Super-lattices as Millimetre-wave devices' Suplattices and Microstructures, Vol 2, Nos 3, 1986.

179

Simple models for high-frequency MESFETs and comparison with experimental results

C.H. Oxley and A.J. Holden

Indexing terms: Computer-aided design, Microwave circuits and networks

Abstract: The paper presents a distributed model for high-frequency MESFETs and compares experimental *S*-parameter measurements to 26 GHz with distributed and lumped models. The concept of distributed effects within a MESFET is used to modify the Fukui noise model, and good agreement has been obtained between high-frequency (35 GHz) noise measurements and the modified Fukui analysis.

1 Introduction

Over the past two decades the f_{max} of the gallium arsenide (GaAs) MESFET has increased from the order of tens of MHz to in excess of 100 GHz. Discrete GaAs devices are now showing good RF performance up to 60 GHz and measurements have been made as high as 115 GHz [1]. The transistors are already finding their way into high frequency systems, for example satellite borne 30/20 GHz transponders, communication and ECM systems. There is also interest in developing the MESFET for millimetric (40–100 GHz) wave operation, and the planar nature of the MESFET makes it very amenable to integration with other circuit elements on GaAs, forming a millimetric microwave monolithic integrated circuit (MMMIC) [2].

With the movement to higher frequency and increased level of integration, there is a requirement to be able to model the active device sufficiently accurately for circuit design and to improve the understanding of the device in order to optimise it further, in particular, for high-frequency operation. This paper will describe in some detail an interpretation of the device as a distributed network, along with some experimental evidence to substantiate this concept.

High-frequency low-noise GaAs MESFETs have been successfully developed at Plessey, Caswell. The transistors were optimised primarily for low-noise operation in *Q*-band (26.5–40.0 Ghz), although gains of 4 to 6 dB would be available at 60 GHz. Fig. 1 shows a photograph of one of the device variants. The use of relatively simple geometry has led to ease of fabrication with the potential for high yields in manufacture. The transistor is fabricated on n^+/n vapour phase epitaxial (VPE) material, which is grown on a high resistivity buffer layer to isolate the active layer from the electrical deleterious effects of the substrate. The device is fabricated using a hybrid photolithography/electron-beam (EB) lithography process; the ohmic source/drain contacts being realised using photolithography, while the 0.25 μm gate length is exposed by electron-beam lithography. The typical measured source resistance and extrinsic transconductance (g_m) are of the order of 0.6 ohms/mm and 250 mS/mm, respectively, although devices with extrinsic transconductances in excess of 320 mS/mm have been measured at room temperature. A summary of the device measured RF performance is shown in Table 1.

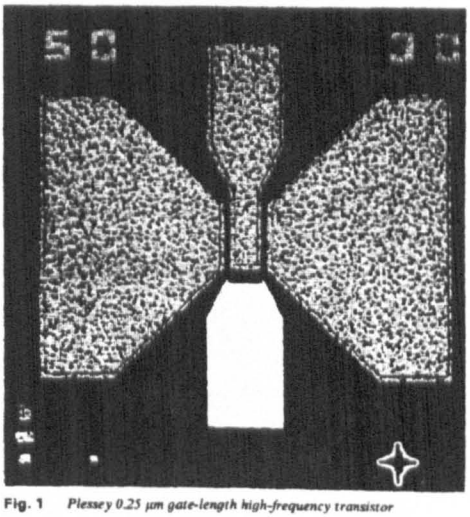


Fig. 1 *Plessey 0.25 μm gate-length high-frequency transistor*

The major electrical parameters which describe the RF performance of a device are, *S*-parameters, gain (*NFG*) and minimum noise figure (NF_{min}). At low frequencies, where geometry of the device is very small compared with a wavelength, simple lumped equivalent circuit models [3] may be used along with the Fukui noise model [4], but at high frequencies, where the device dimensions become comparable to a wavelength, a distributed model may be necessary to describe the transistor more accurately. In

Table 1: Summary of performance for the Plessey high-frequency low-noise GaAs MESFET

Frequency, GHz	NF_{min}, dB	*NFG*, dB	*MAG*, dB
14	1.1	12.0	16.0
18	1.9	10.5	
20	2.0	9.5	
23	2.2	9.5	12.5
28	2.8	7.0	12.5
33*	2.6	5.0	
33	3.7	7.0	
34	—	—	9.5
40	—	—	7.0

* New variant of the transistor

Paper 4831H (E12, E3, C6), first received 24th March and in revised form 1st July 1986

Mr. Oxley is with Plessey Microwave Limited, Wood Burcote Way, Burcote Road, Towcester, Northants NN12 7JS. Dr. Holden is with the Allen Clark Research Centre, Plessey Research (Caswell) Limited, Caswell, Towcester, Northants NN12 8EQ, United Kingdom

practice it has been found that the simple lumped equivalent circuit model can be modified in order to provide an improved fit at higher frequencies (over a finite band), but at the expense of obtaining an acceptable fit at the lower frequencies. The elements also making up this equivalent circuit model often bear little relation to the physical layout of the device. In such cases the lumped models become less useful as tools to understand and optimise the active devices and are at best narrow-band device simulators for use in circuit analysis.

2 Distributed model

At high frequency, new physical effects become important in the device and must be adequately accounted for in the device model. These effects include direct inter-electrode coupling (giving rise to additional parasitic capacitance and mutual inductance), and distributed phase effects (particularly along the conventional 'width' of a MESFET gate). The distributed FET model (DFM) developed at Plessey Research (Caswell) Ltd. (PRCL) is designed to address these two aspects. It is based on the model used by PRCL to describe the travelling-wave FET [5] and travelling-wave amplifier [6].

A unit gate section of a conventional MESFET can be viewed as three couple active transmission lines, which are depicted schematically in Fig. 2. In the DFM, the electrodes are treated as coupled microstrip lines, and an

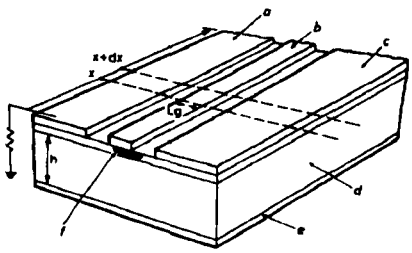


Fig. 2 *Schematic diagram of FET structure as a three-line coupled structure*

a Source
b Gate
c Drain
d Dielectric semi-insulating GaAs
e Ground-plane metallisation
f Active region

extension to the image charge and Green function approach of Silvester [7] is used to calculate the mutual capacitance and inductance matrices. Details of this calculation are published elsewhere [5], and typical matrices for the Plessey high-frequency (Fig. 1) device are shown in Table 2. In simple terms, the FET electrode layout may be treated as five parallel lines on the surface of the semiconductor above a ground plane. The electrodes are depicted (Table 2) as source (S_1), gate (G_2), drain (D_3), gate (G_4) and source (S_5). The capacitance and inductance matrices represent the mutual capacitance and inductance between the five electrodes and from the electrodes to the ground

Table 2A: Calculated capacitance and inductance matrices for the interelectrode coupling on the surface of a MESFET

5 × 5 capacitance matrix (pF/cm)

	S_1	G_2	D_3	G_4	S_5
S_1	1.04	0.309	0.968	0.0135	0.591
G_2	0.309	0.0019	0.527	0.0008	0.0135
D_3	0.96	0.522	0.078	0.527	0.968
G_4	0.0135	0.0008	0.522	0.0019	0.309
S_5	0.59	0.0135	0.968	0.309	1.04

Table 2B

5 × 5 inductance matrix (μH/cm)

	S_1	G_2	D_3	G_4	S_5
S_1	0.0064	0.0046	0.0042	0.0038	0.0032
G_2	0.0046	0.014	0.0060	0.0052	0.0038
D_3	0.0042	0.0060	0.0072	0.006	0.0042
G_4	0.0038	0.0052	0.006	0.014	0.0046
S_5	0.0032	0.0038	0.0042	0.0046	0.0054

S_1 = source electrode
G_2 = gate electrode
D_3 = drain electrode
G_4 = gate electrode
S_5 = source electrode

plane. For example, the element C_{23} is the gate-to-drain inter-electrode capacitance and L_{13} is the mutual inductance between the source and drain lines. The symmetry ensures that the second gate and source have similar interactions, although interactions between the two gates or the two sources are relatively small. As the ground plane is well removed, the inter-electrode effects are largely confined to the surface of the device and hence can be considered to be unaffected by screening or other interactions from the active regions. This is the basis of separation between the active admittance and the inter-electrode admittance. The active elements, particularly the gate-source (C_{gs}) depletion capacitance, dominate the system, and so small errors in the inter-electrode values are not significant. Only in the case of the gate-drain capacitance (C_{gd}) is this not true. Here it was found that the inter-electrode value derived by the method described constitutes almost all the value extracted from *S*-parameter measurements. This suggests that even at low frequencies this inter-electrode term is significant.

Superimposed onto the inter-electrode capacitance and inductance is the active FET device. By limiting considerations to TEM-solutions to the transmission-line problem, the active device can be included as a distributed equivalent circuit added in parallel to the direct inter-electrode coupling. A differential element of this distributed circuit is shown in Fig. 3. This generalised coupled transmission-line

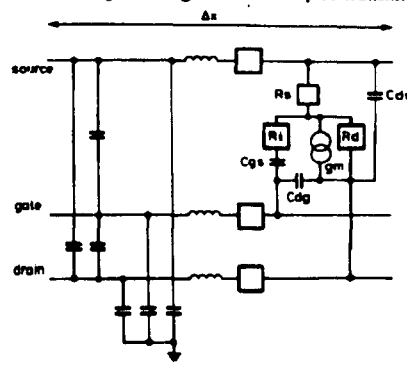


Fig. 3 *Equivalent circuit diagram of a differential element of an active transmission-line system (MESFET)*

problem is solved in the DFM by a matrix generalisation of conventional transmission-line theory [5]. The result is a set of six normal modes, three travelling in each direction along the width of the gate. The problem is also solved in the DFM for a two-gate structure (source-gate-drain-gate-source) by treating it as five coupled active transmission

lines with ten normal modes. This structure is akin to the PI geometry of the Plessey high-frequency transistor (Fig. 1). Further gates may be added as in conventional circuit analysis as direct coupling becomes less important.

Once the normal modes have been found, the boundary conditions on each end of the transmission lines are incorporated. In the DFM these can be 50 Ω terminations, voltage sources or combinations of reactive and resistive networks including sources as specified by the user. With the boundary conditions in place, the currents and voltages at any point on the transmission lines are specified by an appropriate linear combination of normal modes with coefficients fitted to suit the boundary conditions.

With this information, the DFM calculates the *S*-parameters, available gain (MAG), maximum stable gain (MSG), unilateral and current gains, and the input and output impedances of the device.

The appropriate intrinsic device equivalent circuits are obtained from DC measurements and RF measurements at *low* frequency, where distributed effects are likely to be unimportant. A standard topology is used as shown in Fig. 3, and additional source inductance to ground and inter-electrode capacitance can be added if required. Once this low-frequency circuit is treated as distributed ('per unit length') across the gate width, it then becomes applicable to higher-frequency operation.

3 Comparison between experimental *S*-parameters and distributed and lumped models

The *S*-parameters of the Plessey high-frequency device were measured on the HP8510 (26.5 GHz version) and directly compared with the distributed model and a lumped equivalent circuit model derived from *S*-parameter measurements to 12.4 GHz. The plots for S_{11}, S_{22} and S_{21}

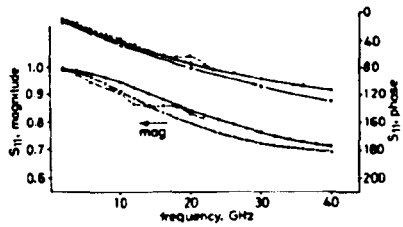


Fig. 4A S_{11} comparison of experiment with lumped and distributed models

▲—▲ experimental
●—● distributed
—+— lumped

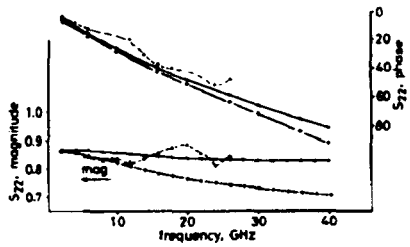


Fig. 4B S_{22} comparison of experiment with lumped and distributed models

▲—▲ experimental
●—● distributed
—+— lumped

(Fig. 4*a*, *b* and *c*) all show an improved fit for the distributed model to high frequencies. The high-frequency gain

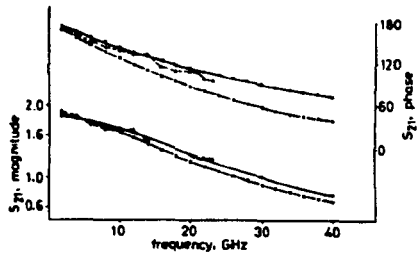


Fig. 4C S_{21} comparison of experiment with lumped and distributed models

▲—▲ experimental
●—● distributed
+— lumped

(maximum available gain ($K \geqslant 1$) and maximum stable gain ($K \leqslant 1$) of the transistor are also calculated. These calculated gains again agree more closely with experimentally measured high-frequency gains ($\geqslant 20$ GHz) when compared with the extrapolated gain values obtained from the simple lumped model.

The DFM can be applied to a wide range of FET structures and has been used to model wide-gate power devices as well as the very high frequency devices discussed here. At high frequency the DFM shows significant deviations from traditional extrapolation theories (6 dB per octave etc.) underlining the possible role of distributed effects in limiting high-frequency performance.

4 Modified Fukui noise model

The other important RF parameter in the design of small signal MESFET devices is the noise figure (NF) of the transistor. An approximate but very useful expression for calculating the minimum noise figure (NF_{min}) of a MESFET is given by Fukui [4], and may be simply written as follows:

$$NF_{min} = 1 + KC_{gs}F2\pi\left[\frac{(RS_1 + RS_2 + RC) + R_g}{g_{m0}}\right]^{1/2}$$

where

C_{gs} = gate-source capacitance
F = frequency
$RS_1 + RS_2 + RC$ = components making up the total source resistance
R_g = gate resistance
g_{m0} = intrinsic transconductance

The above parasitics are shown schematically in Fig. 5.

The coefficient K is empirically derived, and Fukui relates this to material quality. The Fukui equation is an

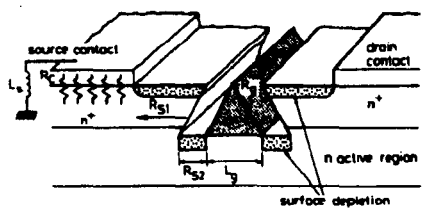


Fig. 5 Schematic diagram of FET showing principal parasitics

approximation of the more general expression given by Pucel [8], and neglects induced gate noise, higher-order terms in frequency and assumes a correlation coefficient close to unity.

The above Fukui equation [4, 9] may be expressed in terms of the geometry and material parameters of the device, as given below

$$NF_{min} = 1 + FKL_g(g_m)[R_C(n^+, G, p) + RS_1(n^+, G, D) + RS_2(n, G, D) + R_g(G, p, F)]^{1/2}$$

where

L_g = gate length as a function of g_m

R_C = contact resistance as a function of carrier concentration, n^+, device geometry, G, and metal resistivity p; RS_1 and RS_2 (see Fig. 5) source resistance components as a function of n^+, n, G and surface depletion, D. R_g, gate resistance as a function of G, frequency F, and p.

If the expression is used to calculate the dependence of noise figure on unit gate width, as a function of frequency, the curves in Fig. 6 are obtained. The analysis indicates a

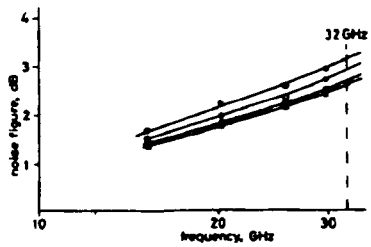


Fig. 6 *Fukui analysis prediction for noise figure for different unit gate width transistors (gate length = 0.3 μm)*

● 100 μm
○ 65 μm
□ 50 μm
▲ 35 μm

very small increase in noise figure, with increasing unit gate width which may be very simply explained by the expected increase in gate resistance, whereas in practice a very different picture emerges, see Fig. 7. The experimental plot was obtained for a number of devices with the same

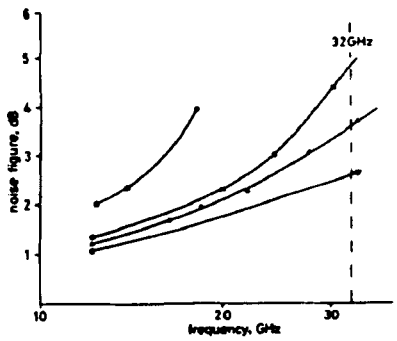


Fig. 7 *Experimental noise figure for different unit gate width transistors (gate length = 0.3 μm)*

● 100 μm
□ 65 μm
▲ 50 μm
■ 35 μm

geometrical layout and gate length (≈0.3 μm), but a range of unit gate widths. The plot indicates that the measured noise figure departs from the Fukui model, and the frequency of departure is related to the unit gate width. The distributed model was used to determine the normal modes for the active device. Each mode has a propagation constant which has a mode velocity associated with it. The dominant modes have similar velocities for the structure considered (Fig. 1) and an average value was taken to give an estimate of the typical wavelength, λ_g, appropriate to the device operation at each frequency. Such a choice is only approximate but was considered adequate, and it was found that the point of departure from the Fukui model appeared to be related to the point where the unit gate width was approximately $\lambda_g/20$, see Table 3. This figure is

Table 3: Frequency of departure from linear dependence of noise figure on frequency for various gate widths. Also shown is the gate width as a fraction of the two principal propagation wavelengths and their average

Unit gate width	Frequency of departure	Slow wave	Fast wave	Average
100 μm	14 GHz	$\lambda_g/7.2$	$\lambda_g/36$	$\lambda_g/21$
65 μm	20 GHz	$\lambda_g/8.0$	$\lambda_g/38$	$\lambda_g/23$
50 μm	26 GHz	$\lambda_g/8.0$	$\lambda_g/38$	$\lambda_g/23$
35 μm	34 GHz	$\lambda_g/8.0$	$\lambda_g/40$	$\lambda_g/24$

often taken as a general criterion [10] for describing the point where a passive component changes from a lumped to distributed description. This simple criterion may be used to modify empirically the Fukui analysis in order to describe the faster increase in noise figure with frequency than is presently predicted. For simplicity, $F_B(W)$ is defined as the frequency at which the experimental results depart from the Fukui analysis, and is a function of unit gate width (W). It was found that the experimental results fit the following modified form of the Fukui analysis:

$$NF_{min} = 1 + F_B(W)C_0 + F - F_B(W)[C_0 + (1 + F_B(W)C_0\,0.23C_1] + (F - F_B(W))^2[(1 + F_B(W)C_0)0.14C_1^2 + 0.23C_1C_0] + \text{Higher-order terms if required}$$

The coefficient C_0 is related to the type of expression originally given by Fukui

$$C_0 = KL_g(g_m)[R_C(n^+, G, p) + RS_1(n^+, G, D) + RS_2(n, G, D) + R_g(G, p, F)]^{1/2}$$

The coefficient C_1 was empirically derived and for gallium arsenide MESFETs was found to be of the order of 0.088 for the condition $F \geq F_B$, otherwise, for $F \leq F_B$, $C_1 = 0$ and the expression returns to the original Fukui equation.

5 Comparison between modified Fukui noise model and experimental results

The analysis has been used and compared with measurements for a number of transistors. Fig. 8 compares the experimental noise figure (NF_{min}) of a Plessey high-frequency device with the modified Fukui analysis, and very good agreement was obtained to high frequencies approaching 40 GHz. The model has also been used to compare with experimental noise figures of other manufacturers devices, which are shown in Table 4.

The form of equation allows optimisation and analysis of different device layouts (material, device layout and

channel geometry) to obtain a minimum noise-figure operation for a particular frequency band or spot frequency. Fig. 9 shows the expected noise performance for a 'PI'

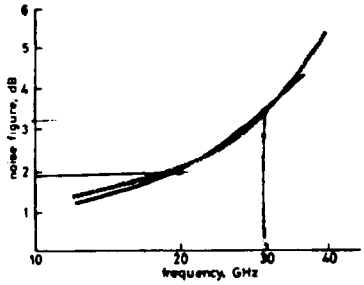


Fig. 8 *Comparison of experimental and theoretical noise characteristics for a 0.3 μm gate-length MESFET*

x — x theoretical
· — · experimental
Device 50 μm unit gate width
100 μm total gate width

	R_i, Ohms	g_m, mS
Predicted	7.1	25
Observed	7.5	23

Table 4: Measured noise performance for a range of reported devices, together with their predicted performance obtained from our model

Device type	Frequency	Measured noise figure	Predicted noise figure
Plessey High frequency FET	33 GHz	3.7 dB	3.8 dB
NEC 673	22 GHz	2.6 dB	2.6 dB
Hughes	30 GHz	2.0 dB	2.1 dB
Plessey high frequency FET (Variant 2)	33 GHz	2.6 dB	2.5 dB
Hughes	60 GHz		5.75 dB

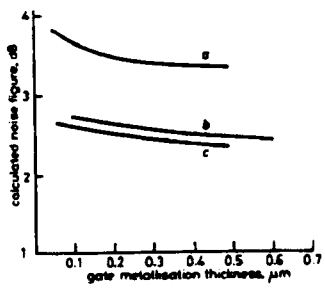


Fig. 9 *Calculated noise figure of a FET as a function of unit gate width and gate metallisation thickness*

a Unit gate width 75 μm
b Unit gate width 50 μm
c Unit gate width 35 μm
Frequency of operation 34 GHz
Gate length 0.3 μm

FET structure as a function of unit gate width and gate metallisation thickness. The analysis indicated that, at least for low-noise small-signal devices, there is little advantage in developing very low resistance, 'T'-profile gate structures. Furthermore, it is of interest to note that if the Fukui factor K is redefined using the recently published work of Cappy [11], to include active material thickness, dielectric constant ε, etc., then the analysis may be used to calculate the minimum noise figure (NF_{min}) for the high electron mobility transistor (HEMT). The model has been used to optimise device geometry for a millimetric frequency HEMT device, the predicted noise performance of the device is shown in Fig. 10.

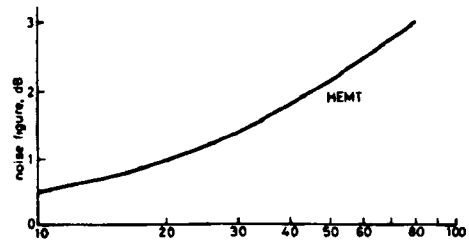


Fig. 10 *Prediction of future state-of-the-art noise figure for millimetric HEMT devices*

Gatelength = 0.2 μm

6 Conclusions

The work presented in this paper indicates that at high frequencies the simple lumped equivalent circuit and Fukui noise models may not be adequate to describe the GaAs MESFET. A distributed model for the MESFET is presented which agrees well with experimental S-parameters up to 26 GHz and high-frequency gain (40 GHz) measurements. A modified form of the Fukui noise model is also presented which has been shown will describe very adequately the minimum noise figure for a GaAs MESFET and HEMT devices at high frequencies.

7 Acknowledgments

Part of this document was carried out with the support of the Procurement Executive, UK Ministry of Defence (Directorate of Components, Valves and Devices) sponsored from the Royal Signals and Radar Establishment. The authors would also like to thank R. Bennett and D. Brambley for the electron beam work, I. Davies and S. Cotton for device fabrication and B. Wheeldon and A. Powell for RF characterisation.

8 References

1 TSERNG, H., and KIM, B.: 'A 115 GHz monolithic GaAs FET oscillator'. GaAs IC Symposium, 12th–14th November 1985, Monterey, California, USA, pp. 11–13
2 KING, B., TSERNG, B.Q., and SHIH, H.D.: '44 GHz monolithic GaAs FET amplifier', *IEEE Trans.*, 1986, EDL-7, (2), pp. 95–97
3 OXLEY, C.H., BUTLIN, R., ARNOLD, J., PEAKE, A., and BENNETT, R.: 'Q-band (26–40 GHz) FETs'. IEDM Digest, Washington, Dec. 1981
4 FUKUI, H.: 'Optimum noise figure of microwave GaAs MESFETs', *IEEE Trans.*, 1979, ED-26, (7), pp. 1032–1037
5 HOLDEN, A.J., DANIEL, D.R., DAVIES, I., OXLEY, C.H., and REES, H.D.: 'Gallium arsenide travelling wave field-effect transistors', *ibid.*, 1985, ED-32, pp. 61–66
6 HOLDEN, A.J., and OXLEY, C.H.: 'Computer modelling of travelling wave transistors'. Proc. Conf. on Simulation of semiconductor devices and processes, Swansea U.K., 9th–12th July 1984, pp. 319–329
7 SILVESTER, P.: 'TEM wave properties of microstrip transmission lines', *Proc. IEE*, 1968, 115, pp. 43–48
8 PUCEL, R.A., BAUS, H.A., and STATZ, H.: 'Signal and noise properties of GaAs microwave MESFETS' *in* 'Advances in electronics and electron physics' (Academic Press, 1975), pp. 195–265
9 HUGHES, A.: 'Fabrication of sub half micron gate length GaAs MESFETs'. 5th Specialist Workshop on Active Microwave Semiconductor Devices, Venice, Italy, October 1975

channel geometry) to obtain a minimum noise-figure operation for a particular frequency band or spot frequency. Fig. 9 shows the expected noise performance for a 'PI'

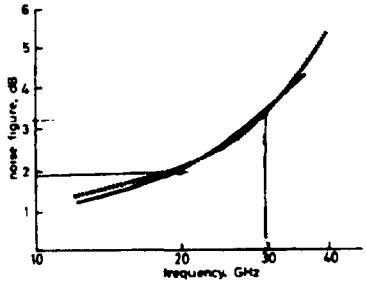


Fig. 8 *Comparison of experimental and theoretical noise characteristics for a 0.3 μm gate-length MESFET*

x — x theoretical
—— experimental
Device 50 μm unit gate width
100 μm total gate width

	R_s Ohms	g_m mS
Predicted	7.1	25
Observed	7.5	23

Table 4: Measured noise performance for a range of reported devices, together with their predicted performance obtained from our model

Device type	Frequency	Measured noise figure	Predicted noise figure
Plessey High frequency FET	33 GHz	3.7 dB	3.8 dB
NEC 673	22 GHz	2.6 dB	2.6 dB
Hughes	30 GHz	2.0 dB	2.1 dB
Plessey high frequency FET (Variant 2)	33 GHz	2.6 dB	2.5 dB
Hughes	60 GHz		5.75 dB

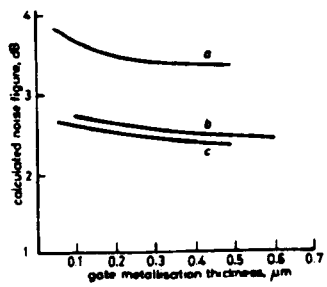


Fig. 9 *Calculated noise figure of a FET as a function of unit gate width and gate metallisation thickness*

a Unit gate width 75 μm
b Unit gate width 50 μm
c Unit gate width 35 μm
Frequency of operation 24 GHz
Gate length 0.3 μm

FET structure as a function of unit gate width and gate metallisation thickness. The analysis indicated that, at least for low-noise small-signal devices, there is little advantage in developing very low resistance, 'T'-profile gate structures. Furthermore, it is of interest to note that if the Fukui factor K is redefined using the recently published work of Cappy [11], to include active material thickness, dielectric constant ε, etc., then the analysis may be used to calculate the minimum noise figure (NF_{min}) for the high electron mobility transistor (HEMT). The model has been used to optimise device geometry for a millimetric frequency HEMT device, the predicted noise performance of the device is shown in Fig. 10.

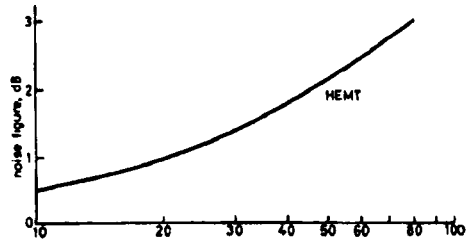


Fig. 10 *Prediction of future state-of-the-art noise figure for millimetric HEMT devices*

Gatelength = 0.2 μm

6 Conclusions

The work presented in this paper indicates that at high frequencies the simple lumped equivalent circuit and Fukui noise models may not be adequate to describe the GaAs MESFET. A distributed model for the MESFET is presented which agrees well with experimental *S*-parameters up to 26 GHz and high-frequency gain (40 GHz) measurements. A modified form of the Fukui noise model is also presented which has been shown will describe very adequately the minimum noise figure for a GaAs MESFET and HEMT devices at high frequencies.

7 Acknowledgments

Part of this document was carried out with the support of the Procurement Executive, UK Ministry of Defence (Directorate of Components, Valves and Devices) sponsored from the Royal Signals and Radar Establishment. The authors would also like to thank R. Bennett and D. Brambley for the electron beam work, J. Davies and S. Cotton for device fabrication and B. Wheeldon and A. Powell for RF characterisation.

8 References

1 TSERNG, H., and KIM, B.: 'A 115 GHz monolithic GaAs FET oscillator'. GaAs IC Symposium, 12th–14th November 1985, Monterey, California, USA, pp. 11–13
2 KING, B., TSERNG, B.Q., and SHIH, H.D.: '44 GHz monolithic GaAs FET amplifier', *IEEE Trans.*, 1986, EDL-7, (2), pp. 95–97
3 OXLEY, C.H., BUTLIN, R., ARNOLD, J., PEAKE, A., and BENNETT, R.: 'Q-band (26–40 GHz) FETs'. IEDM Digest, Washington, Dec. 1981
4 FUKUI, H.: 'Optimum noise figure of microwave GaAs MESFETs', *IEEE Trans.*, 1979, ED-26, (7), pp. 1032–1037
5 HOLDEN, A.J., DANIEL, D.R., DAVIES, I., OXLEY, C.H., and REES, H.D.: 'Gallium arsenide travelling wave field-effect transistors', *ibid.*, 1985, ED-32, pp. 61–66
6 HOLDEN, A.J., and OXLEY, C.H.: 'Computer modelling of travelling wave transistors'. Proc. Conf. on Simulation of semiconductor devices and processes, Swansea, U.K., 9th–12th July 1984, pp. 319–329
7 SILVESTER, P.: 'TEM wave properties of microstrip transmission lines', *Proc. IEE*, 1968, 115, pp. 43–48
8 PUCEL, R.A., BAUS, H.A., and STATZ, H.: 'Signal and noise properties of GaAs microwave MESFETS' *in* 'Advances in electronics and electron physics' (Academic Press, 1975), pp. 195–265
9 HUGHES, A.: 'Fabrication of sub half micron gate length GaAs MESFETs'. 5th Specialist Workshop on Active Microwave Semiconductor Devices, Venice, Italy, October 1975

10 HIRACHI, Y., TAKEUCHI, Y., IGARASHI, M., KOSEMURA, K., and YAMAMOTO, S.: 'A packaged 20 GHz 1 watt GaAs MESFET with a novel via-hole plated heat-sink structure', *IEEE Trans.*, 1984, MTT-32, (3), pp. 309–316

11 CAPPY, A., VANOVERSCHELDE, A., SCHORTGEN, M., VERSNAEYEN, C., and SALMER, G.: 'Noise modelling in sub micrometer gate two dimensional electron gas field effect transistors', *IEEE Trans.*, 1985, ED-32, pp. 2787–2796

Erratum

KAJFEZ, D., WHELESS, W.P., and WARD, R.T.: 'Influence of an airgap on the measurement of dielectric constant by a parallel plate dielectric resonator', *IEE Proc. H, Microwave, Antennas & Propag.*, 1986, 133, (4), pp. 253–258

The following should be inserted above eqn. 20:

$$S_L^2 = \frac{2}{1 + \left[\frac{x_{mn} L}{p\pi a}\right]^2}$$

for the TER_{mnp} modes, and

4920H

allows us to estimate a maximum operating frequency as in a simple inverter: it can be expressed as

$$F_{max} = \frac{1}{2t_{pdd}}$$

t_{pdd} being the propagation delay time of a simple inverter with a fan-out N. In this dynamic divider $N = 2$, so at a frequency of 8 GHz the corresponding t_{pdd} is of the order of 62 ps.

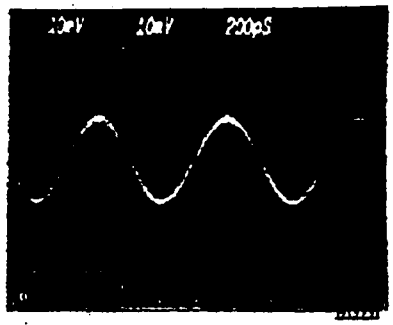


Fig. 2 *Output waveform of dynamic divider-by-3 operating at input frequency of 7 GHz*

Taking into account the propagation delay time measured on the ring oscillator test circuits, fabricated on the same wafer ($t_{pd1} = 40$ ps), we can deduce an useful relationship between t_{pdd} and t_{pd1} which is characteristic of our planar technology:

$$t_{pdd} = 1{\cdot}5t_{pd1}$$

This relation confirms our previous results concerning the fan-out influence on t_{pd} of ring oscillators fabricated on two-dimensional electron gas structures.[9]

So it appears that the performances of this new type of dynamic divider could be increased with the optimisation of the fan-out of the output stage or with that of the propagation delay time: according to the different data in the literature (10 to 20 ps),[5–7] surpassing 10 GHz in the very near future seems to be quite reasonable. In fact, the most interesting point is that, theoretically, toggle frequencies as high as 30 GHz could be expected in dividers based on the original proposed geometry.

Conclusion: A new design of dynamic frequency divider has been tested on MBE-grown layers by using a DCFL technology. An 8 GHz input frequency has been achieved in spite of poor electrical characteristics; the total power dissipation measured at this frequency has been found to be as low as 23·5 mW. If we take into account these first encouraging results, we can conclude that this new type of design has great potential for future microwave systems applications.

Acknowledgments: The authors would like to thank J. F. Rochette and P. Delescluse for their assistance with the MBE growth, J. Jarry for his help in measurements at high frequencies, and M. Gloanec and M. Belmas for many helpful discussions.

P. N. TUNG
J. CHEVRIER

21st April 1986

Thomson Semiconducteurs
Route Départementale 128, BP 48
91401 Orsay, France

References

1 PHAM, N. T.: 'Porte logique à coincidence'. French patent no. 84-19194, 1984; Thomson reference number: 53988y
2 DELAGEBEAUDEUF, D., LAVIRON, M., DELESCLUSE, P., PHAM, P. N., CHAPLART, J., and LINH, N. T.: 'Planar enhancement mode two-dimensional electron gas FET associated with a low surface potential', *Electron. Lett.*, 1982, 18, pp. 103–104
3 PHAM, N. T., DELESCLUSE, P., DELAGEBEAUDEUF, D., LA... CHAPLART, J., and LINH, N. T.: 'High-speed low-power DC... planar two-dimensional electron gas FET technology', ... 18, pp. 517–518
4 TAKADA, T., SHIMAZU, Y., and YAMASAKI, K.: 'A 2 Gb/s th... GaAs digital time switching LSI using LSCFL'. IEEE M... posium, technical digest, 1985, pp. 22–26
5 SHOKI, T., YAMASAKI, K., OKAFUNEI, K., and ODAWARA, E.: ... 10 GHz frequency dividers with GaAs advanced SAINT ... bridge technology', *Electron. Lett.*, 1986, 22, pp. 68–69
6 CIRILLO, N. C., ABROKWAH, J. K., FRANSEN, A. M., and VO... 'Ultra-high speed ring oscillators based on self-align... modulation-doped n^+ (Al, Ga)As/GaAs', *ibid.*, 1985, ... 772–773
7 LEE, C. P., HOU, D., LEE, S. J., MILLER, D. L., and ANDERS... 'Ultra-high speed digital integrated circuits using GaAs/... high mobility transistors'. IEEE GaAs IC symposium, ... digest, 1983, pp. 162–165
8 'Bell Labs builds 5·8 ps transistor', *Electronics*, 1985, 16, p. ...
9 CHEVRIER, J., and PHAM, N. T.: ESPRIT 232, Final report, 19...

MODIFIED FUKUI MODEL FOR HIGH-FREQUENCY MESFETs

Indexing terms: Modelling, Field-effect transistors

The letter will describe a modified form of the Fuku... model to describe the high-frequency noise perform... MESFETs.

Introduction: A number of variants of high-frequenc... noise (GaAs) FETs have been designed and fabricate... electron-beam lithography to define the gates at ... Caswell. The RF performance of one of the variants o... FETs is summarised in Table 1. When the m...

Table 1

Frequency	NF_{min}	NFG	MAG
GHz	dB	dB	dB
14	1·1	12·0	16·0
18	1·9	10·5	—
20	2·0	9·5	—
23	2·2	9·5	12·5
28	2·8	7·0	12·5
32*	2·6	5·0	—
33	3·4	7·0	—
34	—	—	9·5
40	—	—	7·0

* New variant of the transistor

minimum noise figure (NF_{min}) is plotted against frequen... directly compared with the predicted noise figure given ... Fukui noise expression,[3] the experimental and pr... values for NF_{min} depart noticeably at high frequencies (F...

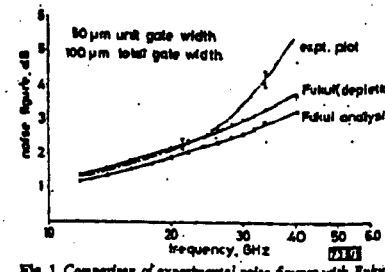


Fig. 1 *Comparison of experimental noise figures with Fukui ... high frequencies, for a 0·3 μm-gate-length Plessey MESFET*

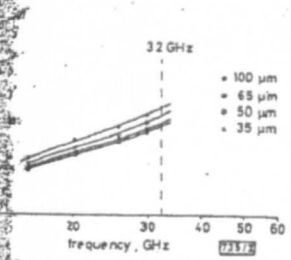
analysis: The Fukui noise equation is an ... but very useful expression for calculating the ... figure (NF_{min}) of a MESFET and may be ... as follows:

$$NF_{min} = 1 + KC_{gs}F2\pi\left[\frac{(RS_1 + RS_2 + RC) + R_g(W)}{g_{mo}}\right]^{1/2}$$

... gate-source capacitance, F = frequency, RS_1 + ... are components making up the total source ... $R_g(W)$ = gate resistance (W = unit gate width) and ... transconductance.

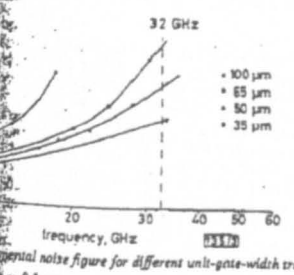
... constant K is empirically derived, which Fukui relates ... quality. The Fukui equation is an approximation ... general expression given by Pucel,[4] and neglects ... noise, higher-order terms in frequency and ... correlation coefficient close to unity.

... above expression is used to calculate the dependence ... figure on unit gate width, as a function of frequency, ... in Fig. 2 are obtained. The analysis indicates a very



... analysis prediction for noise figure for different unit-gate ... ... = 0·3 μm

... in noise figure with increasing unit gate width, ... very simply explained by the expected increase ... resistance, whereas in practice a very different picture ... (see Fig. 3). The experimental plot was obtained for a



... mental noise figure for different unit-gate-width transistors ... = 0·3 μm

... Plessey devices with the same geometrical layout ... length (≈0·3 μm) but a range of unit gate widths. ... indicates that the measured noise figure departs from ... model, and the frequency of departure is related to ... gate width. A distributed model[5–7] was used to deter- ... velocity modes within the device structure, and it ... that the point of departure from the Fukui model ... be related to the point where the unit gate width ... approximately $\lambda_g/20$. This figure is often taken as a ... criterion for describing the point where a passive com- ... changes from a lumped to distributed description. This ... was used to modify the Fukui analysis empiri- ... describe the faster increase in noise figure with fre- ... currently predicted. For simplicity $F_g(W)$ is ... frequency at which the experimental results ... the Fukui analysis, and is a function of unit gate width W. It was found that the experimental results fit the following modified form of the Fukui analysis:

$$NF_{min} = 1 + F_g(W)C_0 + FC_0\sqrt{F_g(W)[C_0 + (1 + F_g(W)C_0)0{\cdot}23C_1]} + [F - F_g(W)]^2\{[1 + F_g(W)C_0]0{\cdot}14C_1^2 + 0{\cdot}23C_1C_0\} + \text{higher-order terms if required}$$

The coefficient C_0 is related to the type of expression originally given by Fukui:

$$C_0 = KC_{gs}\sqrt{2\pi\left[\frac{RS_1 + RS_2 + RC + R_g(W)}{g_{mo}}\right]^{1/2}}$$

The coefficient C_1 was empirically derived and for gallium arsenide MESFETs was found to be of the order of 0·088 for the condition $F \geq F_g$; otherwise for $F \leq F_g$, $C_1 = 0$ and the expression returns to the original Fukui equation. A more complete treatment of the above analysis is given in Reference 7.

Comparison with experiment: This analysis has been used and compared with measurements for a number of transistors. These are given first in Fig. 4, which compares the experimen-

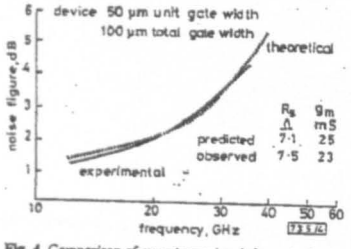


Fig. 4 *Comparison of experimental and theoretical noise characteristics for a Plessey 0·3 μm-gate-length MESFET*

tal noise figure (NF_{min}) of a Plessey high-frequency transistor with the modified Fukui analysis, and secondly in Table 2, where the analysis is compared with the experimental noise figure of other manufactured devices. From these results it can be seen that good agreement was obtained to frequencies approaching 40 GHz.

Conclusions: A simply empirically modified form of the Fukui noise model has been presented which shows good agreement with experiment to frequencies approaching 40 GHz. It is expected that the analysis may be used to describe more adequately the expected noise performance of MESFETs in the millimetric frequency range.

Acknowledgments: Part of this research was carried out with the support of the Procurement Executive, UK Ministry of Defence (Directorate of Components, Valves & Devices) sponsored from the Royal Signals & Radar Establishment. The authors would also like to thank R. Bennett and D. Brambley

Table 2

Device type	Frequency	Measured noise figure	Predicted noise figure
	GHz	dB	dB
Plessey high-frequency FET (variant 1)	32	3·7	3·8
NEC 673	22	2·6	2·6
Hughes	30	2·0	2·1
Plessey high-frequency FET (variant 2)	33	2·6	2·5
Hughes	60	—	5·75

for the electron beam work, I. Davies and S. Cotton for device fabrication, and B. Wheeldon and A. Powell for RF characterisation.

C. H. OXLEY† 24th April 1986
A. J. HOLDEN

Plessey Research (Caswell) Ltd.
Caswell
Towcester
Northants NN12 8EQ, United Kingdom

† Now with Plessey Microwaves Ltd.

References

1 OXLEY, C. H., *et al.*: 'Q-band (26–40 GHz) FETs'. IEDM digest, Washington, Dec. 1981
2 OXLEY, C. H.: 'Millimetre MESFETs'. Plessey Research, Caswell, Annual review, 1985
3 FUKUI, H.: 'Optimum noise figure of microwave GaAs MESFETs', *IEEE Trans.*, 1979, ED-26
4 FUCHS, B. A., RAUR, M. A., and STATZ, H.: 'Signal and noise properties of GaAs microwave MESFETs', *Adv. Electron. & Electron Phys.*, 1975
5 HOLDEN, A. J., DANIEL, D. R., DAVIES, I., OXLEY, C. H., and REES, H. D.: 'Gallium arsenide travelling wave field-effect transistors', *IEEE Trans.*, 1985, ED-32, pp. 61–66
6 HOLDEN, A. J., and OXLEY, C. H.: 'Computer modelling of travelling wave transistors'. Proc. of conf. on simulation of semiconductor devices and processes, Swansea, UK, 1984, pp. 319–329
7 OXLEY, C. H., and HOLDEN, A. J.: 'Simple models for high-frequency MESFETs and comparison with experimental results', *IEE Proc. H, Microwaves, Antennas & Propag.*, to be published

SLOW-WAVE POWER DIVIDER

Indexing terms: Microwave devices and components, Power dividers, Microstrip lines

A novel power divider made of a coupled slow-wave microstrip line is proposed and its characteristics discussed. The difference between the attenuation constants for even and odd modes in a coupled slow-wave microstrip line are successfully used to eliminate a resistor.

Introduction: Although a number of slow-wave structures have been proposed and analysed,[1,2] the application of these transmission lines has been limited in a certain area.[3] The circuit performance is deteriorated by the large transmissions line loss due to a lossy dielectric layer. However, the attempt to apply the attenuation characteristics of a slow-wave microstrip line has recently been reported and the voltage-controlled attenuator has been predicted.[4] In this letter a novel power divider made of a coupled slow-wave microstrip line[5,6] is proposed and frequency characteristics are calculated. The numerical predictions are compared with the conventional lossless power divider.[7] The power divider proposed here is based on the difference between the attenuation losses of two orthogonal modes. The proposed structure has the following features: (i) the length of the power divider is very small because of slow-wave effect; (ii) no resistors are needed for isolation; (iii) regardless of coupling characteristics of coupled line, the frequency bandwidth of this power divider is larger than that of the noncoupled lossless power divider because of transmission-line loss.

Analysis: The circuit configuration of the coupled slow-wave microstrip line power divider is shown in Fig. 1a. The coupled microstrip line is formed on three-layer substrate. The symmetrical power divider is analysed by the method of even- and odd-mode excitations of ports 2 and 3.[5] Figs. 1*b* and *c* show the equivalent circuits by even- and odd-mode excitations, respectively. In this Figure, Z_{even}, Z_{odd}, γ_{even} and γ_{odd} are the characteristic impedance and propagation constant of even and odd modes, respectively. The voltage reflection coefficients Γ_e and Γ_o are written as follows:

$$\Gamma_e = \frac{Z_e \cosh \gamma_e l}{3Z_e \cosh \gamma_e l + 2\sqrt{(2)}Z_e \sinh \gamma_e l}$$

$$\Gamma_o = \frac{Z_{oo} \sinh \gamma_o l - Z_o \cosh \gamma_o l}{Z_{oo} \sinh \gamma_o l + Z_o \cosh \gamma_o l}$$

where $Z_{oo} = 2Z_o$. According to Reference 6, the attenuation constant of odd mode α_{odd} can be larger or smaller than that of even mode α_{even}. At the centre frequency, eqn. 2 is reduced as $(Z_{oo}/Z_o - \tanh \alpha_o l)/(Z_{oo}/Z_o + \tanh \alpha_o l)$. When the attenuation constant or the line length becomes large, Γ_o is reduced to $(Z_{oo}/Z_o - 1)/(Z_{oo}/Z_o + 1)$, e.g. the reflection constant is independent of $\alpha_o l$ and this value is determined by the ratio

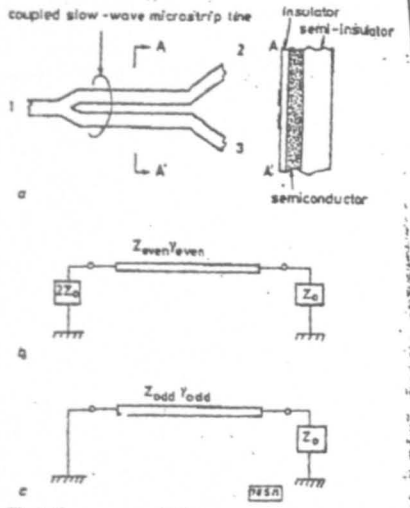


Fig. 1 *Slow-wave power divider*
a Circuit configuration of slow-wave power divider
b Equivalent circuit of even-mode excitation
c Equivalent circuit of odd-mode excitation

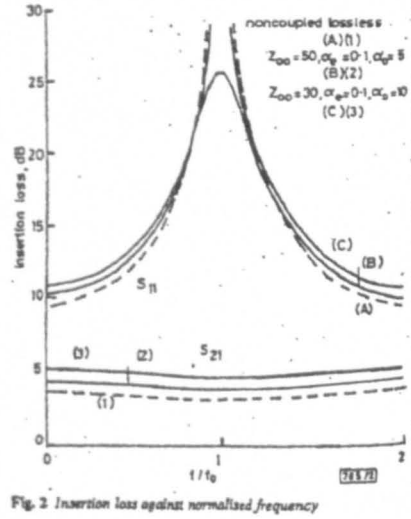


Fig. 2 *Insertion loss against normalised frequency*

198

An extract from the

Allen Clark Research Centre 1985 Annual Review

Millimetric Wave Gallium Arsenide FETs

by C H Oxley

Introduction. The first microwave gallium arsenide (GaAs) metal Schottky barrier field-effect transistor (MESFET) was fabricated and measured in 1965 at the Allen Clark Research Centre. ***Fig. 1*** shows a photograph of one of these early devices, [1] which has a gate-length in excess of 10μm and a cut-off frequency (f_T) of the order of tens of MHz. Since then device design and technology have progressed very rapidly, and transistors with f_Ts well in excess of 50GHz are fabricated as a matter of routine. They have gate-lengths of less than 0.3μm, measured noise figures of under 3.0dB in mid C-band (26.5-40GHz), and are finding applications in many high-frequency (20-60GHz) systems. They are competing effectively, in some cases, with the more traditionally used two terminal solid state devices (Gunn oscillators, gallium arsenide and indium phosphide reflection amplifiers) in the millimetric wave-bands.

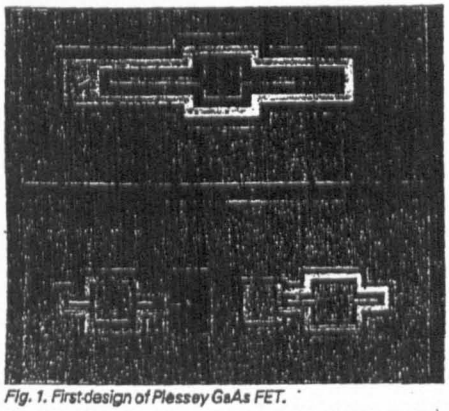


Fig. 1. First design of Plessey GaAs FET.

The MESFET is the most versatile active solid state device in current microwave design. It is used in low noise and high power amplifiers, oscillators, mixers, switches and more recently in travelling wave structures which give the capability of multi-octave bandwidths (0.1-50GHz) [2]. The planar nature of the MESFET makes it very amenable to integration with other circuit elements on GaAs, forming microwave monolithic integrated circuits (MMIC) [3]. The continuous drive to increase the frequency of operation of the MESFET, as well as lowering the noise figure and increasing its output power capability, is leading to device and circuit design refinements, and the use of new technologies, for example electron beam (EB) lithography, ion-beam milling, molecular beam epitaxy

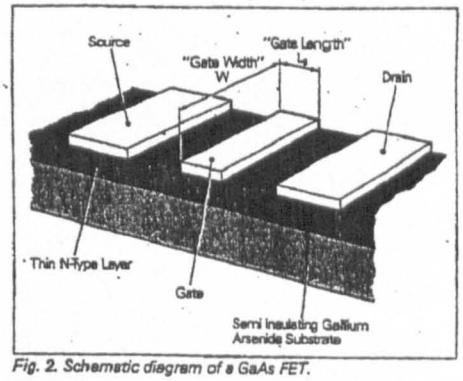


Fig. 2. Schematic diagram of a GaAs FET.

(MBE) and metal-organic chemical vapour deposition (MOCVD). For this reason it is essential that a close working relationship exist between the device technologist and the circuit designer in order to obtain the best device for a particular application. No single device structure or combination of material parameters can produce a transistor that satisfies the high-frequency, low noise, wide-bandwidth and output power requirements of all applications.

The High Frequency MESFET. A simple schematic diagram of a MESFET is shown in *Fig. 2*. The basic cell consists of three electrodes which are termed the source, gate and drain. In FET terminology the shorter dimension of the gate is known as the gate-length (L_g) and the longer dimension as the gate width (W). The gate-length determines the frequency of operation whilst the gate width determines the impedance and output power capability of the device.

The cut-off frequency (f_T) of operation of the MESFET may be very simply thought of as being inversely proportional to the carrier transit time under the gate-electrode. Therefore to obtain high-frequency operation, a short gate-length and a semiconductor material with a high carrier mobility is required. Gallium arsenide (GaAs) and related III-V materials (gallium indium arsenide, (GaInAs), and gallium aluminium arsenide, (GaAlAs), all exhibit a high carrier mobility, at least five times greater than that of silicon (Si), and are therefore chosen for microwave devices. The more fundamental aspects of the behaviour of III-V compound semiconductors have been discussed in a previous number of this review [4].

190

As the gate length is shortened, the thickness of the semiconductor active region has to be reduced, and therefore the carrier concentration increased, in order to preserve the pinch-off characteristics (which determine the voltage on the gate that reduces the source to drain current to zero) of the transistor. The reduction in the active semiconductor thickness leads to higher parasitic source and drain resistances, and higher gate capacitance, and also places the following very stringent requirements on the semiconducting material:–

a) An abrupt step in carrier concentration at the interface to maintain the transconductance (g_m) of the transistor.

b) A low number of growth imperfections at the interface to minimise degradation of the carrier mobility.

c) A non-conducting substrate to prevent leakage current (I_s) past the gate via the substrate. This leakage current dominates the performance of very small geometry transistors.

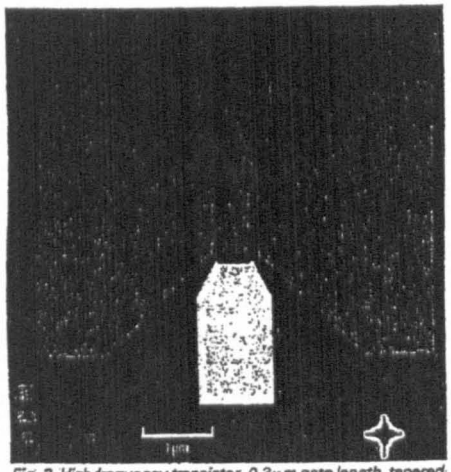


Fig. 3. High frequency transistor. 0.3μm gate length, tapered electrodes, on-chip identification.

In practice, transistors (*Fig. 3*) with gate lengths of 0.3μm have been fabricated on an n-type active layer grown by vapour phase epitaxy (VPE) on a high resistivity (10^7 ohm.cm.) buffer layer. The buffer layer isolates the n-active layer from imperfections within the substrate. The transistor has a measured transconductance of 240mS/mm, an f_T of greater than 50GHz and good pinch-off characteristics, indicating good material quality. It is expected that further improvements will be obtained by using the metal-organic chemical vapour deposition (MOCVD) or molecular beam epitaxy (MBE) growth technique to obtain steeper carrier concentration profiles at the interface and much thinner active semiconductor layers. These growth technologies will also enable the active region to be grown on a wider band-gap material, for example gallium aluminium arsenide (GaAlAs) or as a super-lattice structure to act as a potential well, and to minimise the leakage of carriers into the substrate. Improved DC characteristics close to

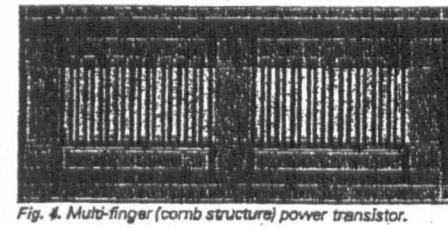


Fig. 4. Multi-finger (comb structure) power transistor.

pinch-off have already been obtained by using a GaAlAs buffer region to minimise the substrate leakage.

The gate-width, W, of the transistor will determine both its input impedance and its output power capability. To a first approximation the f_T of the device is invariant with gate-width, since both the input capacitance and transconductance (g_m) increase linearly with gate-width. However, the gate capacitance has to be reduced when the frequency is increased in order to maintain a suitable input impedance. Also the physical size of the transistor needs to be sufficiently small in order to maintain phase coherence throughout the structure. This latter criterion becomes increasingly important as the frequency of operation is raised and largely determines the output power capability of millimetre wave devices. A useful guide to the maximum output power of a MESFET is 1.0W per millimetre of gate width. Simple calculations suggest that by using a compact multi-finger structure, similar to that of an X-band power FET (*Fig. 4*), 500mW of output power could be obtained at 40GHz.

Simple Models. The apparently simple matter of reducing the gate lengths to increase the frequency of operation of a transistor requires the skills of both device designer and technologist to minimise parasitics whilst maintaining a structure which can be easily fabricated. The latter requirement is important when considering high volume manufacture in which processing costs and yields are of paramount importance.

Valuable information on the effects of device parasitics on r.f. performances (noise figure and gain) can be obtained using relatively simple semi-empirical models.

A useful expression for the noise figure of a MESFET has been devised by Fukui [5]:–

$$NF_{min} = 1 + K L_g f [g_m (R_s + R_g)] 1/2$$

Where K is the fitting factor representing the quality of the channel material, approximately 2.3 for GaAs; L_g is the gate length; f is the frequency; g_m is the transductance, R_s is the parasitic resistance between source and gate; R_g is the parasitic gate resistance.

From the equation it can be seen that a short gate length is needed for low noise as well as for high frequency operation. The reduction in thickness of the active region required by high frequency operation will increase the source to gate resistance (R_s) and therefore the noise figure. The following techniques can be used to minimise R_s:–

(a) A reduction in the distance between the source electrode and gate stripes. How far this can be carried will

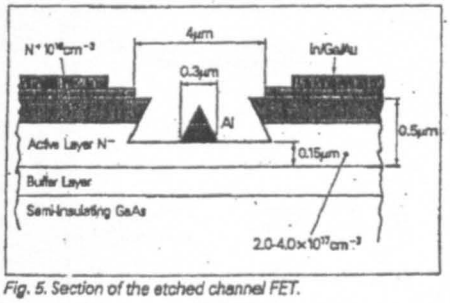


Fig. 5. Section of the etched channel FET.

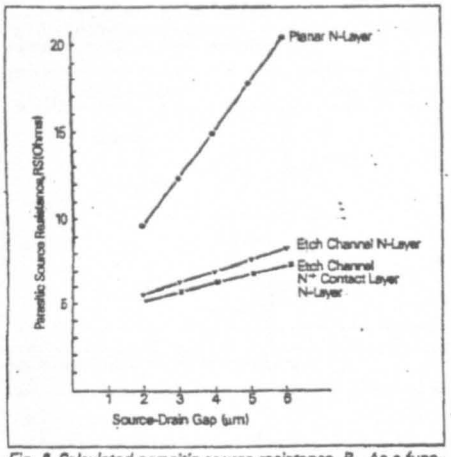


Fig. 6. Calculated parasitic source resistance, R_s, As a function of source-drain gap, for different geometries.

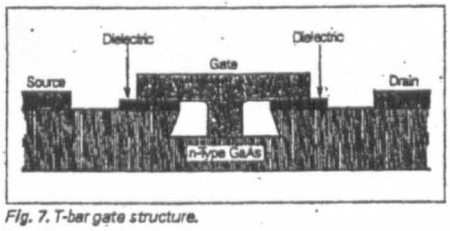


Fig. 7. T-bar gate structure.

be limited by an accompanying increase in the inductive and capacitive parasitics.

(b) The use of a thick active layer and the etched gate channel structure shown in *Fig. 5*. This both decreases R_s and gives good pinch-off characteristics.

(c) The inclusion of a high carrier concentration (10^{18} atom/cm^3) contact layer grown on top of the active region (*Fig. 5*), which effectively extends the source and drain contacts to the edge of the etched channel.

The relative effectiveness of the above techniques in reducing the source resistance is shown in *Fig. 6*.

The parasitic gate resistance (R_g) is the resistance associated with the metallised gate stripe and it will increase significantly as the gate length is reduced. It can be reduced, while maintaining total gate width, by splitting the gate into a number of stripes which are then paralleled together to form a comb structure (*Fig. 4*). Alternatively a T-gate technology may be adopted. The T-gate consists of a thick metal bar fabricated on the gate which is usually supported by a dielectric. (*Fig. 7*).

Both approaches have been used in different devices. For a power transistor a large gate width is required with a compact geometry to minimise phase differences across the device, which is particularly important with increasing frequency, so that the comb structure has been adopted in this case. For the travelling wave transistor (linear gate transistor, LGT) [2] a single gate is required, leading to the use of the T-gate technology which allows devices with gate lengths of 0.6μm to be fabricated with parasitic gate resistances of 3 to 10 ohm/mm.

To enable the Fukui noise theory to be successfully used in the design of high frequency low noise MESFETs it has been expanded to include the skin-effect within the gate stripe, the surface depletion of the GaAs and also a term to take into account frequency distributed type of effects within the structure. A schematic of a cross-section of the FET and associated parasitics is shown in *Fig. 8*. These parasitics can be directly related to device geometry and material parameters as shown in the following expression:–

$$NF_{min} = 1 + KL_g(g_m)\,[R_c(n^+, G, \rho) + R_{s1}(n^+, G, D) + R_{s2}(n\pm, G, D) + R_g(G, \rho, f)]^{1/2} + Dist[f, G]$$

L_g gate length is a function of g_m; R_c, contact resistance as a function of carrier concentration, n^+, device geometry, G, and metal resistivity ρ; R_{s1} and R_{s2} (see *Fig. 8*) source resistance components as a function of n^+, n, G and surface depletion, D. R_g, gate-resistance as a function of G, frequency, f, and ρ; Dist,distributed effects as a function of f and G.

It has been found that the expression gives very good agreement with noise measurements, over a wide frequency range. An example is given in *Fig. 9* which compares the predicted and measured noise-figure up to 33GHz for a Plessey 0.3μm gatelength transistor. Simi-

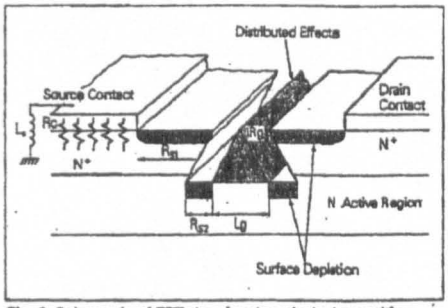


Fig. 8. Schematic of FET showing the principal parasitics.

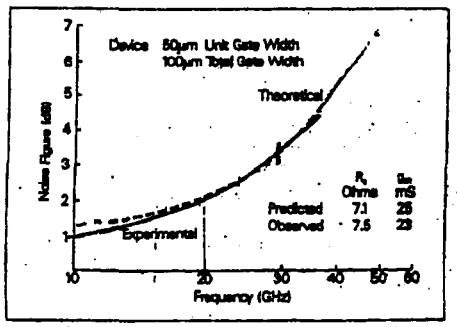


Fig. 9. Comparison of experimental and theoretical noise characteristics for a 0.3μm Gate Length FET.

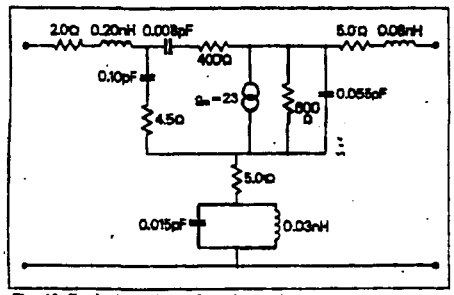


Fig. 10. Equivalent circuit for HF transistor.

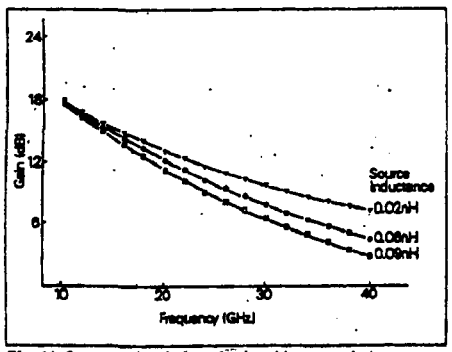


Fig. 11. Computed variation of gain with source inductance.

lar agreement can also be obtained for a wide range of devices. This relatively simple model is a very powerful tool for the design of high frequency, low noise MESFETs.

The gain of the transistor can be investigated by using a simple equivalent circuit model (*Fig. 10*) for the transistor. The magnitudes of the parameters making up the equivalent circuit may be directly obtained from the above device model, and/or experimentally determined from DC and small signal S-parameter measurements. For a given device geometry the circuit indicates that the most important parasitic in obtaining high frequency gain is the source inductance, L_s. *Fig. 11* shows how the gain of the transistor varies with both frequency and the parasitic source to ground inductance. This parasitic can be reduced by using multiple bond-wires, source wrap-round or via contacts.

The Plessey Q-Band Transistor. The design aspects discussed have been applied in the realisation of the 0.3μm gate-length transistor, shown in *Fig. 3*. The transistor has been optimised primarily for operation in Q-band (26.5 – 40.0GHz) although its measured f_T of 50GHz would enable gains of 4 to 5dB to be obtained at 60GHz. The use of a simple geometry has led to ease of fabrication with the potential for high yields in manufacture. The unit gate width, W, is determined by the onset of transmission line effects along the metallised gate stripe. *Fig. 12* shows a plot of the computed NF_{min} at 24GHz as a function of metallisation thickness and unit

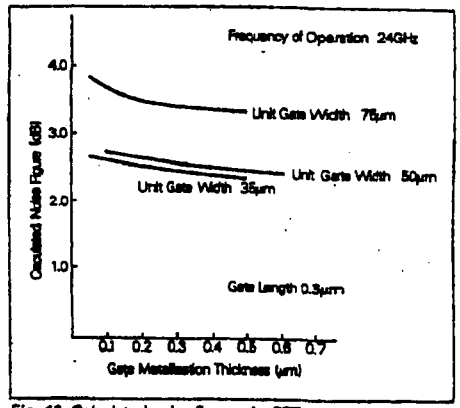


Fig. 12. Calculated noise figure of a FET as a function of unit gate width and gate metallisation thickness.

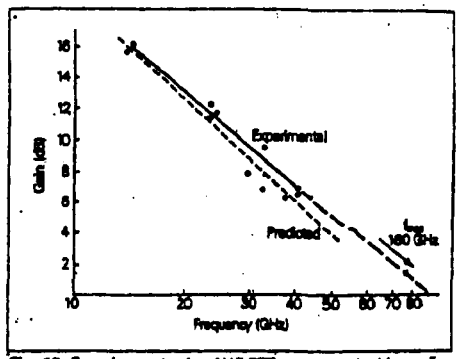


Fig. 13. Experimental gain of HF FET compared with predictions from the equivalent circuit model.

gate width. The results indicate a substantial increase in NF_{min} for unit gate widths of 75μm which is accounted for by the onset of distributed effects. Hence to obtain low noise and high-frequency of operation the unit gate width has been optimised for operation in Q-band. To minimise the source resistance, R_s, a thin highly conductive (10^{18} carriers/cm^3) GaAs layer has been used in an etched channel technology. The typical measured R_s component is 0.8ohms/mm and a maximum g_m of 270mS/mm has been recorded. The source to ground parasitic inductance has been minimised by designing tapered source electrodes (***Fig. 3***) which allow the use of short multiple bond wires or tapes. A comparison between the experimentally measured gain and those predicted using the simple equivalent circuit model is shown in ***Fig. 13***.

A summary of the RF performance of this transistor is given in Table 1.

Freq.(GHz)	NF_{min}(dB)	MFG(dB)	MAG(dB)
14	1.1	12.0	16.0
18	1.9	10.5	-
20	2.0	9.5	-
23	2.2	9.5	12.5
28	2.8	7.0	12.5
33	3.4	7.0	10.5
40	-	7.0	-

Table 1. RF performance of Plessey Q-band transistor.

Improved variants of this transistor are now giving NF_{min} of less than 3.0dB above 30GHz.

Fabrication. The current Plessey high-frequency MESFETs are fabricated on n+/n VPE material, which is grown on a high-resistivity buffer layer to isolate the active region from the electrically deleterious effects of the substrate. The first stage of the process is to electrically isolate the device areas on the wafer. This is carried out by defining the areas using conventional photolithography followed by chemically etching the gallium arsenide back to the substrate to form islands of active (n+/n) semiconductor (mesas). The ohmic source drain contact patterns are then printed using photolithography and the contact metals are deposited by thermal evaporation. The wafer is then ready for defining the sub-micrometre gate stripes using electron-beam (EB) lithography.

A Cambridge Instrument's EB machine has been used to expose the gate patterns. The beam diameter is less than 0.1μm which gives the potential of exposing very small feature sizes well outside the scope of the normal ultra-violet photolithographic system [8].

The channel is then etched chemically, and the gate metals deposited by evaporation. The resulting unit is approximately 300μm square so that there is the possibility of some 15,000 devices from a 5cm diameter GaAs wafer.

With so many devices per wafer, the transistors have been given individual identification numbers (see ***Fig. 3***), and are automatically DC probed using a computer controlled probe station. The major parameters monitored are I_{dss} (saturation current), V_p (pinch-off voltage), V_B (drain-gate breakdown voltage) and g_m (transconductance) of the transistor. The data collected may be

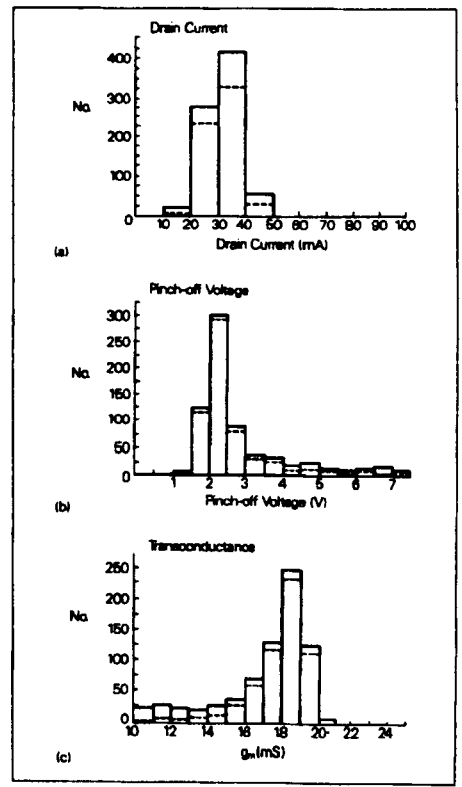


Fig. 14. Histograms of DC characteristics of a batch of HF FETs.

displayed in many forms giving valuable information regarding the uniformity of any one parameter across the wafer and the number of devices which fall in a given band of DC parameters. ***Fig. 14*** shows typical histogram plots for some of the probed DC parameters (I_{dss}, V_p and g_m) for a batch of high-frequency transistors. This is a very powerful technique as devices can be selected on both the DC data and on visual appearance.

Applications. The advances in device performance are offering the circuit designer the opportunity to develop new components for a variety of millimetric wave system applications; in particular, narrow band (10-15%) low noise amplifiers for space-borne applications, at present between 20 and 50GHz, and wide band units for communication and electronic counter-measure requirements. The continuous improvements in noise performance and frequency of operation are now directly challenging the more traditional parametric and travelling wave tube amplifiers. A number of devices are under development both at the ACRC and at the

manufacturing division, Plessey III-V, whilst their use in systems is being pursued by Plessey Microwave (PMWL).

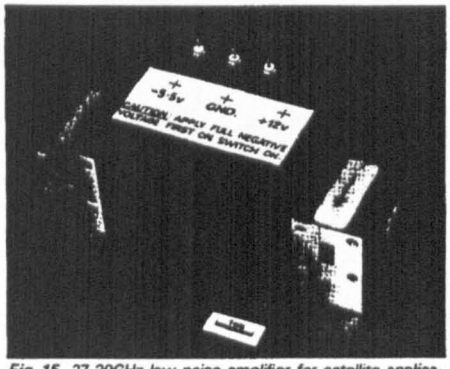


Fig. 15. 27-30GHz low noise amplifier for satellite applications.

Fig. 15 shows a photograph of a complete high gain low noise (27 – 30.0GHz) amplifier for satellite transponders. The amplifier consists of six stages directly cascaded together, which is known as a 'single-ended' configuration. A low noise figure is obtained over a limited band-width of approximately 10%. Each of the amplifier stages uses a high-frequency device mounted in the well on a ridge. This arrangement minimises the critical parasitic source inductance by keeping the source to ground bond wires short. The microstrip matching circuits have been fabricated on quartz substrates to minimise r.f. losses. Microstrip E-probe to waveguide transitions, *Fig. 16*, have been used at both the input and output ports of the amplifier. To maintain a low voltage standing wave ratio (VSWR) miniature waveguide isolators have been utilised. *Fig. 17* shows the transitions and the geometrical configuration of the amplifier stages, each giving a gain of approximately 6.0dB. As the unit is required to operate over an extensive temperature range(−50 to + 55°C) and the linear gain of a MESFET changes by approximately 0.015dB/°C, a temperature compensating circuit has been developed. This adjusts the negative bias on the gates of the transistors so as to compensate for the change of gain with temperature. The fully temperature compensated amplifier response is shown in *Fig. 18*. The gain variation is less than 2.0dB over −55 – +50°C temperature range. The noise-figure is less than 6.0dB at room temperature, and it is to be expected that this will be reduced to well below 6.0dB using a new variant of the HF transistor which is under development.

State of the art single-stage low noise modules have also been designed for use in future inter-satellite communication links. A photograph of the 23GHz module is shown in *Fig. 19*. Again quartz substrates have been used and the matching circuits designed using small-signal device S-parameters. A lumped element bias-filter has been found to give very good HF R.F. rejection. The frequency response for both 23 and 32GHz modules are shown in *Fig. 20* (a) and (b). The respective

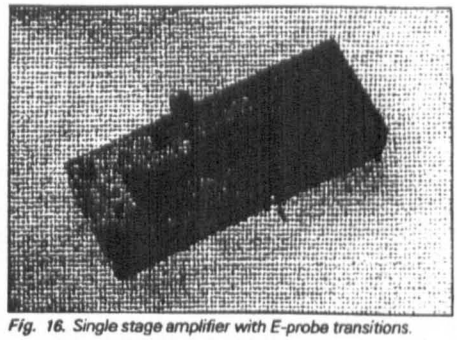


Fig. 16. Single stage amplifier with E-probe transitions.

Fig. 17. 27-30GHz amplifier showing 6 cascaded stages and E-probe transitions.

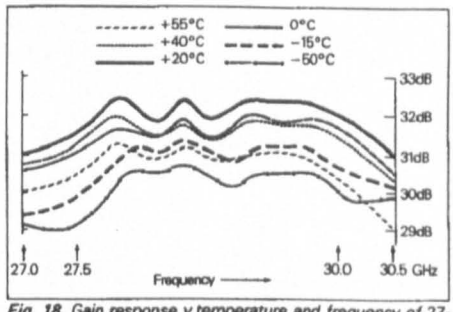


Fig. 18. Gain response v.temperature and frequency of 27-30GHz amplifier.

noise figures are 2.4dB and 4.0dB. For many of these applications substantial improvement in the noise performance can be obtained by cooling. The above 23GHz modules have been cooled to −77°C with a resulting noise figure of about 0.8dB.

The above applications only represent a small fraction of the potential uses of the transistor. For instance the inherent wide-band capability of these devices would allow the design and operation of wide-band amplifiers, 18-40GHz, with predicted gains of 30-40dB. Even grea-

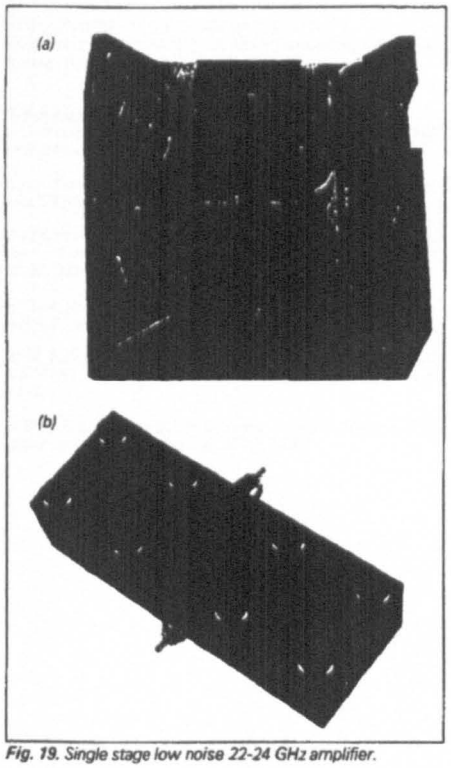


Fig. 19. Single stage low noise 22-24 GHz amplifier.

(a) Internal view showing the device mounted in the centre in a well on the ridge.

(b) Complete module with E-probe transitions.

ter band-widths 0.1-50GHz are feasible using travelling wave circuit configurations. The present device structure in a single-ended amplifier configuration is capable of giving output powers in excess of 13dBm at 30GHz. If a balanced configuration is used (the input signal is split into two and each half is amplified and then recombined at the output) powers in excess of 16dBm are already feasible. These units will challenge the travelling wave tube amplifiers (TWTs), as they offer higher reliability, lower noise, small size and operation from low voltage DC supplies.

The other potential area of application is in HF oscillators. With device f_{max}'s already in excess of 100GHz, and the potential of it being raised above 200GHz, fundamental millimetric oscillators delivering several milliwatts of output power are feasible. The planar technology of the MESFET will also enable it to be more easily incorporated into integrated circuits than the counterpart two terminal devices, thereby paving the way to millimetric MMIC circuits.

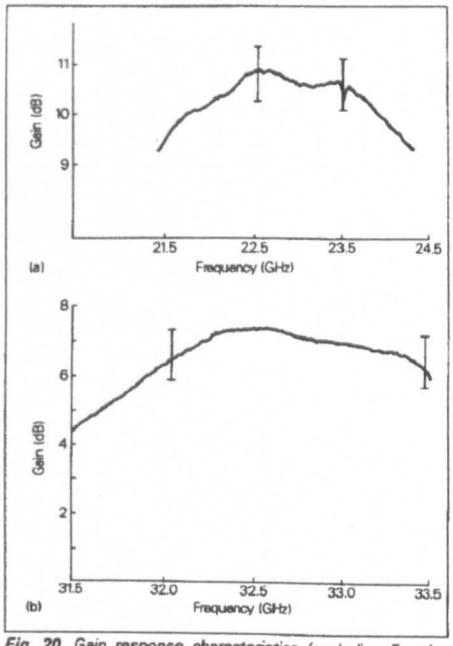


Fig. 20. Gain response characteristics (excluding E-probe transitions) (a) 23GHz, (b)32.5GHz module.

Future. In the last two decades MESFET design and technology has increased the f_T of the transistor by almost a factor of 500, from 100MHz to 50GHz. In the next decade new materials and device designs will lead to f_Ts well in excess of 100GHz.

The new ternary materials, GaInAs and GaAlAs are already being grown and incorporated in devices using metal-organic chemical vapour deposition and molecular beam epitaxy. Their higher carrier mobilities alone will raise the frequency capability of MESFETs, as is confirmed by current results.

Perhaps the area where the greatest strides will be seen will be in the use of ternary compounds in new device designs, for example the HEMT (high-electron mobility transistor), the HJBT (heterojunction bipolar transistor) and the preparation of superlattices, which are fully described in another article (Quantum Well Devices, by Buus, Robbins and Holden) in this number of the Annual Review.

Acknowledgements. Part of this development was carried out with the support of the Procurement Executive, Ministry of Defence (Directorate of Components, Valves and Devices) sponsored from the Royal Signals and Radar Establishment, and also of Intelsat and the European Space Association ESA. The author would like to thank the many people who have contributed in this area over a number of years, in particular R. Bennett and D. Bramley for the electron beam work, I. Davies for

device technology, A. Powell for RF characterisation and J. Arnold for many useful discussions. He would also like to acknowledge the early pioneering work of D. Parker, A.J. Waller and J.A. Turner.

References.

1. J. Turner, 'Gallium Arsenide Transistors: Power at Higher Frequencies'. Systems Technology, Oct. 1981.

2. A.J. Holden and C.H. Oxley, 'Travelling Wave Gallium Arsenide Transistors', A.C.R.C. Ann. Rev. pp 89-96, 1984.

3. R.S. Pengelly, 'GaAs Monolithic Microwave Integrated Circuits – Their impact on future systems'. A.C R.C. Ann. Rev. pp 69-80, 1984.

4. D.M. Brookbanks. Millimetre Wave Solid State Devices. A.C.R.C. Ann. Rev. pp 35-42, 1981.

5. H. Fukui, 'Optimum Noise Figures of Microwave GaAs MESFETs'. IEEE Trans. Electron Devices ED-26$_{(7)}$, 1032, 1979.

6. D.R. Brambley and R.H. Bennett, 'Electron Beam Lithography'. A.C.R.C. Ann. Rev. pp 67-73, 1982.

Fig. 1 shows the structure used. The epitaxial layer has been grown by LPE with a doping level in the active base layer of $n = 1 \times 10^{16}$ cm^{-3}. The emitter and collector areas have been implanted with Be ions with an energy of 200 keV and a dose of 10^{13} cm^{-2} and of 30 keV with 3×10^{13} cm^{-2} in addition to obtain a low resistive contact layer. The base area has been protected during implantation with 700 nm pyrolitic SiO_2 and 1 μm photoresist. The 1 μm implantation mask was fabricated by optical lithography and dry etching for removing the SiO_2 from the emitter and collector area.

The lateral straggling of the implanted ions, which is about 0·2 μm[5] and the diffusion during the annealing process reduces the base width to about 0·5 μm. This value is derived from profile measurements using the Van der Pauw/Hall method in combination with the differential etching technique,[6] assuming that the straggling and diffusion are isotropic. Depth profiles of Be implanted GaAs layers after annealing at 700 C and 800 C for 1/2 h compared with calculated profiles are seen in Fig. 2.

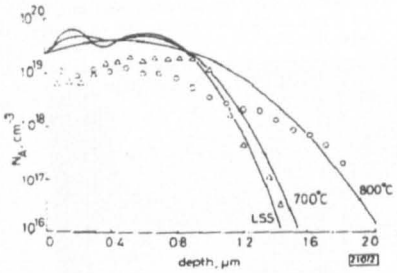


Fig. 2 *Depth profile of electrical active Be atoms (symbols) implanted in GaAs compared with calculated profiles (drawn lines, diffusion constants, see Reference 4)*

Be + GaAs
200 keV, 3×10^{13} cm^{-2}
+ 50 keV, $1·5 \times 10^{13}$ cm^{-2}
△ T_A = 700 C, t_A = 30 min
○ T_A = 800 C, t_A = 30 min

To reduce the vertical injection of holes from the emitter area into the substrate (base), protons have been implanted through the metallised emitter and collector areas to insulate the emitter-substrate interface (crossshadowed area in Fig. 1). During the implantation the base area and the emitter and collector areas immediately adjacent had been protected by a photoresist/Au layer, which has been removed after implantation by lift-off technique. The Au-layer was deposited by electroplating with a thickness of about 1 μm.

First *I/V* characteristics are shown in Fig. 3. The current gain is about 0·5 in the common emitter configuration. For this device the annealing temperature was 700°C for 1/2 h. The vertical to lateral area ratio, which has been 210:1 before isolation implantation, was reduced to 10:1 by proton bombardment.

A strong decrease in current gain is observed at high collector current level. Rey[7] has explained this effect by the resistance of the narrow base region between emitter and collector. A decrease in lateral injection of holes takes place caused by the debiasing of the lateral junction.

An improvement in current gain will be obtained by further reducing the area of the parasitic emitter-substrate diode or by introducing a barrier, like a heterojunction, with higher turn on voltage for this parasitic diode.[8]

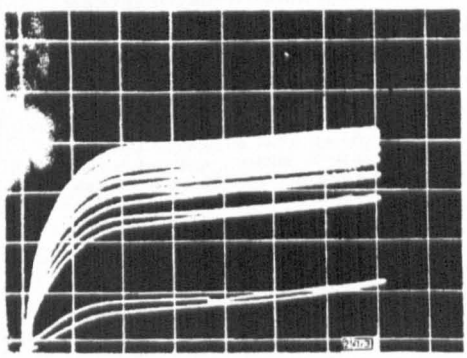


Fig. 3 *I/V characteristics of an ion-implanted pnp GaAs transistor*
(Vertical: 5 μA/div., horizontal: 2 V/div., 10 μA/step, β = 0·5/div.)

Acknowledgments: The authors wish to thank J. Knauf for growing the LPE layers and D. Dunkman for implantation. The work has been supported by the German Research Council SFB 202.

H. KRÄUTLE
P. NAROZNY
H. BENEKING

Institute of Semiconductor Electronics
Aachen Technical University
Templergraben 55, D-5100 Aachen, W. Germany

5th February 1982

References

1 BERGER, H. H., and WIEDMANN, S. K.: 'Merged transistor logic (MTL)—A low-cost bipolar logic concept', *IEEE J. Solid-State Circuits*, 1972, **SC-7**, pp. 340–346
2 BERGER, H. H., and WIEDMANN, S. K.: 'Advanced merged transistor logic by using Schottky junctions', *Microelectronics*, 1976, **7**, pp. 35–42
3 BENEKING, H., GROTE, N., ROTH, W., SU, L. M., and SVILANS, M. N.: 'Realization of a bipolar GaAs/GaAlAs Schottky-collector transistor'. Inst. Phys. Conf. Ser. 56, 1981, pp. 385–391
4 ZÖLCH, R., RYSSEL, H., KRANZ, H., REICHL, H., and RUGE, I.: 'Implantation of Be, Cd, My and Zn in GaAs and $GaAs_{1-x}P_x$'. Proc. international conference on ion implantation in semiconductors', Boulder, Colorado USA, Aug. 9–13, 1976
5 LINDHARD, J., SCHARFF, M., and SCHIOTT, H. F.: 'Range concepts and heavy ion ranges', *Mat.-Fys. Medd. Dan. Vidensk. Selsk.*, 1963, **33**, p. 39
6 ESTEVE, J., PONSE, F., and BACHEM, K. H.: 'Simple and rapid determination of carrier concentration and mobility profiles in GaAs', *Thin Solid Films*, 1981, **82**, pp. 287–292
7 REY, G.: 'On the variation of gain in lateral transistors with bias current', *Solid-State Electron.*, 1967, **10**, pp. 112–114
8 KROEMER, H.: '(Invited) heterostructures for everything: Device principle of the 1980's, *Jpn. J. Appl. Phys.*, 1981, **20**, Suppl. 20-1, pp. 9–13

0013-5194/82/060259-02$1.50/0

Q-BAND (26–40 GHz) GaAs FET SINGLE-STAGE AMPLIFIER

Indexing terms: Semiconductor devices and materials, Field-effect devices

The high-frequency *S*-parameters of a 0·3 μm-gate-length GaAs FET have been measured and compared with the device equivalent circuit model. From the data a *Q*-band single-stage low noise (3·1 dB) amplifier was designed.

Introduction: To design high-frequency (*Q*-band) gallium arsenide (GaAs) FET amplifiers it is necessary to measure the device *S*-parameters in order to realise the input and output equalising networks. This letter presents measured S_{11} and S_{22} parameters of the 0·3 μm-gate-length GaAs FET to frequencies beyond 30 GHz, and these are compared with the *S*-parameters derived using an equivalent-circuit model for the 0·3 μm device. Reasonable agreement was found between the theoretical and experimentally measured *S*-parameters. The *S*-parameters were then used to design distributed input and

output matching networks for amplifier operation at approximately 29 GHz. A resulting single-stage amplifier module gave a measured 3·1 dB noise figure at 27·5 GHz, with an associated gain of greater than 6·0 dB.

Device design and fabrication: To realise a high-frequency (Q-band) GaAs FET the gate length is reduced to the submicron region, and the device parasitics minimised. The principal parasitics are source and drain resistances, gate electrode losses and source inductance. The source and drain resistances were minimised by using an etched channel technology and an N^+ contact layer.[1] The gate length was 0·3 μm, and the contact consisted of an aluminium-based Schottky fabricated on epitaxial N-type GaAs with a carrier density $\simeq 2{\cdot}0 \times 10^{17}$ cm^{-3}. To limit the RF losses in the gate electrode, a unit gate width of 50 μm was adopted. Fig. 1 shows a photograph of the high-frequency FET. It consists of a single-cell orthogonal structure. The 100 μm total gate width gives acceptable high-frequency input and output impedances. To minimise the source bond inductance, the device was designed with trapezium shaped source pads, allowing the bonding of multiple wires or single wide-tapes.

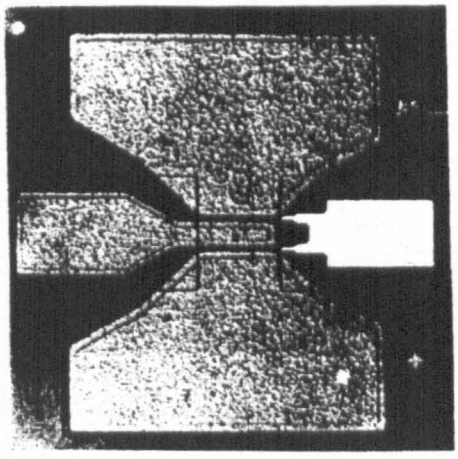


Fig. 1 *Photograph of high-frequency FET*

A hybrid fabrication process was adopted[2,3] to combine the speed of photolithography with the high resolution[2] of electron-beam (EB) lithography. Standard photolithography processing was used to fabricate the ohmic source and drain contacts, and to define the mesa isolation areas with EB technology being used to fabricate the gate and pad structures.

Circuit: The device S-parameters were measured to 18 GHz using a Hewlett Packard automatic network analyser. For these measurements the device was mounted on a metal post, which was inserted through a ceramic substrate, the gate and drain device contacts being bonded to 50 Ω microstrip lines fabricated on the ceramic substrate. De-embedding techniques were then employed to derive the chip S-parameters. The average data from a number of measurements led to the derivation of the unilateral device model. Using the technique of Hower and Bechtel,[4] DC measurements of source (R_s), drain (R_D) and intrinsic (R_I) resistance were also made. These values along with the information from the unilateral model have led to the realisation of a full equivalent-circuit model[5] for the 0·3 μm-gate-length orthogonal EB FET. Fine adjustment to the circuit parameters were made by comparison of derived S-parameters with the measured average S-parameters to 18 GHz. Some difficulties were experienced in obtaining good phase correlation for the S12 parameter.

The model was used to extrapolate the S_{11} and S_{22} parameters to beyond 30 GHz. The predicted high-frequency S-parameters were then checked using slotted-line measurements. For these measurements the FET was mounted in a quartz microstrip circuit, with waveguide 22 to microstrip transitions. This test jig and microstrip test circuit have already been adequately described in References 5 and 6. The measurement reference plane was taken as the interface between the microstrip line and the waveguide taper transition, thus eliminating the effects of the waveguide taper from the characterisation. Also this interface allows the manufacture of a reliable reference short-circuit with a measured VSWR of greater than 100. De-embedding of the device chip from the microstrip circuit was carried out using the Itoh and Mittra spectral domain analysis[7] and the effect of the enclosure wall of the jig on the microstrip-line was taken into account. The Itoh and Mittra analysis was used as it was not dependent on empirically derived dispersion relationships and therefore should be valid for any substrate and to high frequencies. Fig. 2 shows the comparison between the measured and extrapolated S_{11} and S_{22} parameters. From the plot good agreement was obtained below 18 GHz as expected, and reasonable agreement was obtained at high frequencies, giving credence to the equivalent-circuit model.

The high-frequency S-parameters were used to design input and output distributed equalising networks for devices operating at 29 GHz. The circuits were fabricated on 0·381 mm-thick crystalline quartz, and the device mounted on a ridge as in Reference 5. Waveguide 22 to microstrip

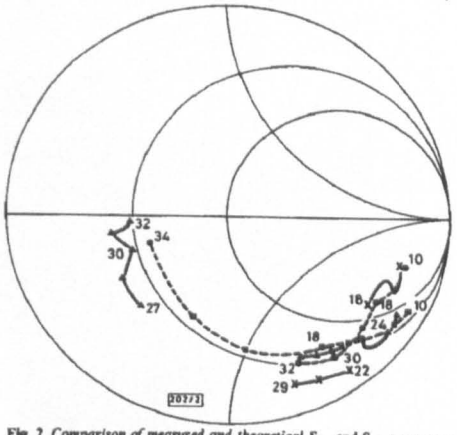


Fig. 2 *Comparison of measured and theoretical S_{11} and S_{22} parameters between 10 and 32 GHz for 0·3 μm EB device structure*

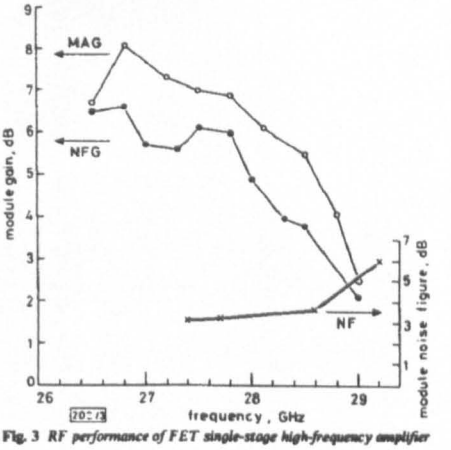


Fig. 3 *RF performance of FET single-stage high-frequency amplifier*

transitions were again utilised.

Fig. 3 shows the operation of the amplifier module, excluding the losses of the waveguide 22 to microstrip transitions. At 27·5 GHz a measured noise figure of 3·1 dB with approximately 6·4 dB of associated gain was obtained. The measured maximum gain was greater than 8·0 dB. The centre frequency of the module was slightly lower than expected and this was attributed to an *S*-parameter measurement accuracy of ± 10 and the requirement for accurate high-frequency microstrip discontinuity characterisation. The present matching circuits were designed using only simple low-frequency discontinuity corrections, which may no longer be valid at the high frequencies.

Conclusions: A 0·3 μm GaAs FET amplifier module has been measured at *Q*-band frequencies, with a measured noise figure of 3·1 dB and an associated gain of 6·4 dB. These figures show the potential of the 0·3 μm EB FET at high frequencies.

Acknowledgments: Part of this work was carried out with the support of Procurement Executive, Ministry of Defence, sponsored by DCVD and ESA. The views expressed are those of the authors only. The authors would like to thank colleagues at Caswell, in particular R. Butlin and J. Arnold, for many valuable discussions.

C. H. OXLEY
A. H. PEAKE
R. H. BENNETT
Allen Clark Research Centre
Plessey Research (Caswell) Ltd
Caswell, Towcester, Northants, NN12 8EQ, England

3rd February 1982

References

1 BUTLIN, R. S., *et al.*: 'J-band performance of 300 mm gate-length GaAs FET'. Proc. IEDM, Washington, 1978
2 BUTLIN, R. S., *et al.*: '200 nanometre gate-length FETs'. Proc. of Cornell electrical engineering conf., Vol. 6, 1977
3 BENNETT, R. H., *et al.*: 'Sub-micron fabrication techniques'. Colloquium on electron beam lithography—The impact on microelectronics', Digest 1980/5, 31 Jan. 1980
4 HOWER and BECHTEL: 'Semiconductors and semimetals' *in* 'Applications and devices, Part A' (Academic Press, 1971, Vol. 7)
5 OXLEY, C. H., *et al.*: 'Q-band (26–40 GHz) FETs'. IEDM digest, Washington, Dec. 1981
6 ARNOLD, J., and BUTLIN, R. S.: 'Extended frequency range GaAs MOSFETs using 0·3 micron gate-lengths'. EMC, Amsterdam, Sept. 1981
7 ITOH, T., and MITTRA, R.: 'Spectral domain approach for calculating the dispersion characteristics for microwave lines', *IEEE Trans.*, 1973, MTT-21
8 OXLEY, C. H., *et al.*: 'Q-band microstrip techniques'. IEE Colloquium Digest, January 1982 (to be published)

0013-5194/82/060260-03$1.50/0

LOW-THRESHOLD CURRENT CW OPERATION OF MULTIPLE INFIL BURIED HETEROSTRUCTURE 1·3 μm GaInAsP LASERS

Indexing terms: Lasers, Semiconductor lasers

1·3 μm buried-heterostructure lasers with CW threshold currents as low as 19 mA have been fabricated using a multilayer infil structure. This technique significantly reduces the alignment tolerances necessary for low-threshold BH laser fabrication. Single transverse and longitudinal mode operation is observed for active layer widths below 3·5 μm.

Introduction: Lasers operating at wavelengths of 1·3 and 1·5 μm are suitable sources for single-mode fibre-optic telecommunication systems. Buried-heterostructure lasers offer the advantage over other forms of isolation of excellent electrical and optical confinement within the active stripe, resulting in low-threshold currents and stable single-mode operation. However, the conventional buried-heterostructure[1,2] can be difficult to fabricate, since its operation is critically dependent on the *p* infil layer thickness. Fig. 1 shows the additional leakage through an InP *p-n* junction that arises if the *p* infil is too thick, and the *n-n* short can arise if the *p* infil layer is too thin.

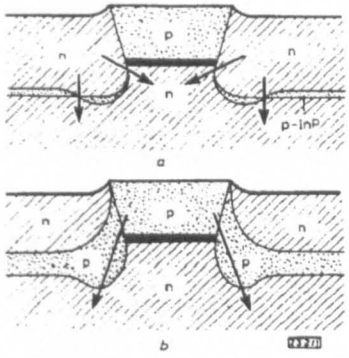


Fig. 1 *Leakage current in buried-heterostructure lasers*
a Isolation layer too thin
b Isolation layer too thick

We report here fabrication and operation of CW 1·3 μm lasers utilising the multiple layer infil,[3] as shown schematically in Fig. 2. Here we arrange for one or more reverse-biased *p-n* junctions to lie below the level of the active region, to ensure minimal leakage regardless of the actual alignment of the infil with respect to the active layer. We believe this technique promises a high yield process for low-threshold current laser fabrication. Lasers with CW room-temperature thresholds as low as 19 mA with stable single transverse and longitudinal modes have been fabricated by this technique.

These results are a considerable advance over preliminary results reported earlier.[3]

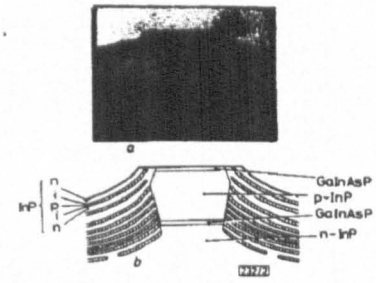


Fig. 2 *SEM (a) and structure (b) of multiple infil laser*

Fabrication: 1·3 μm emitting double-heterostructure laser slices were grown on (001) Sn-doped InP substrates using two-phase liquid phase epitaxy (LPE) with a cooling ramp of 0·3°C/min and an active-layer growth temperature of 640°C. The slices were RF sputtered with silicon nitride which was subsequently plasma-etched to leave various width stripes parallel to ⟨110⟩.

After Br-MeOH etching to form reverse-entrant mesas slices were infilled with a sequence of alternate thin *p*-type (Zn ≃ 1 × 10^{18}) and *n*-type (Ge ≃ 1 × 10^{18}) InP layers. Use of a rotary slider mechanism in the LPE system enabled growth of a large number of *p-n* junctions by switching the slice between melts. To prevent melt carry-over giving rise to intermelt

ITT Colloquium
April '82.

Q-BAND MICROSTRIP TECHNIQUES

C.H. Oxley, J. Arnold and J. Sparrow

INTRODUCTION

High frequency microstrip techniques are being developed to be used with small-signal gallium arsenide FETs, to realise low noise, high gain Q-band amplifier modules.

The microstrip circuits being developed are required to have low r.f. transmission loss. Accurate modelling of the circuits is also necessary to allow de-embedding of the device chip S-parameters from the microstrip circuit, leading to the subsequent design of matching networks. The exactness of the design would be particularly important for the realisation of high-frequency monolithic circuits.

MICROSTRIP DISPERSION MODEL

An initial literature survey on high frequency analytical techniques and measured data for applications beyond 20 GHz, concluded that there was little available information, for example the Getsinger (2) model relies on polynomial curve fitting to measured data below 18 GHz and only on alumina substrates. Therefore the extrapolation of data to higher frequencies, or the use of the equation for other microstrip substrates could lead to erroneous results. Hence the more general ITOH and MITTRA spectral domain model was adopted as it was expected to be valid for any microstrip substrate and to high frequency operation. Figure 1 compares the theoretical effective dielectric constant for the Itoh and Mittra, Getsinger and Edwards and Owens (3) dispersion models applied to a 50 ohm microstrip line on alumina ($\varepsilon_r = 9.8$). The three models were in reasonable agreement below approximately 20 GHz, and as expected the degree of dispersion and agreement between the models greatly improved as the substrate layer thickness was reduced. Simple ring resonator experiments were carried out on 0.635 mm thick alumina, in order to determine the dispersion relationship. The finite thickness of the metallisation pattern was taken into account by calculating the effective line-width for the ring resonator. Exceptionally good agreement was obtained with the Itoh and Mittra model.

The effective dielectric constant for a 50 ohm line on crystalline quartz was computed using the Itoh and Mittra model. Again the values for the effective dielectric constant were determined by ring resonator experiments and reasonable agreement was found. The coefficients of the Getsinger expression were then modified in order to fit the results to those obtained from the Itoh and Mittra model. This comparison is shown in Figure 2, and demonstrates that the modified Getsinger equation will adequately describe the dispersion characteristics of a microstrip line fabricated on a quartz substrate.

Plessey Research (Caswell) Limited, Allen Clark Research Centre, Caswell, Towcester, Northants.

200

The dimensions of the enclosure in which the microstrip circuit is placed should be arranged so that box resonances are prohibited in the frequency band required at high frequencies this often means that the enclosure walls will be sufficiently close to the microstrip line to perturb the propagation constant. The analysis indicated that the lid of the enclosure had little effect upon the effective permittivity of the line, whereas the width dimension had a large influence upon the effective permittivity of the line (Fig. 3).

A theoretical investigation of the r.f. transmission loss of different substrates in particular alumina, quartz and gallium arsenide at high frequencies was undertaken. The analysis included conduction losses, dielectric losses, and losses due to substrate surface roughness. The conduction loss equations were based on the work of Pucel (4), but the surface resistance expression was modified, using the work of Sobel and Caulton (5), to allow for a two-layer metallisation scheme, in order to investigate the effect of the seed-layer on the r.f. transmission loss characteristics. The dielectric losses were computed using the formulation given by Schneider (6), and in this analysis the effective dielectric constant was provided by the Itoh and Mittra model. The loss mechanism caused by surface roughness of the substrate was provided by the expression given by Morgon (7). The computed r.f. losses were checked against published experimental data (8) for a 40 ohm line fabricated on a 0.203 mm thick GaAs substrate and measured to frequencies approaching 40 GHz (Figure 4). These loss figures were compared with the exact loss analysis of D. Meshekar-Syahkal et al in which the perturbation theory and the Itoh and Mittra dispersion model were used. The agreement with the simpler loss analysis was within approximately 14% at 20 GHz and above.

The comparison of microstrip losses for various microstrip substrates were compared by computing r.f. losses/wavelength, since the final designed matching networks will be dependent on electrical length.

Quartz substrates showed the lowest r.f. transmission losses in comparison with alumina and gallium arsenide substrates. The analysis indicated that for minimum loss on quartz the seed-layer metallisation thickness is required to be less than 1000Å and the surface roughness of the substrate better than 5.0 micro-inch CLA. The lower dielectric constant of quartz allowed a high circuit to substrate thickness aspect ratio to be realised. This was found particularly useful for the realisation of low VSWR microstrip to waveguide transitions.

TRANSITIONS

Coaxial SMA to microstrip launchers may be used to frequencies approaching 25 GHz. For frequencies above 25 GHz other forms of transitions have to be considered. To make r.f. connection to the microstrip circuit operating in the frequency band 26 to 40 GHz, a waveguide 22 to microstrip transition was utilised. After consideration of the r.f. performance capabilities and realisability of stepped waveguide transformers, cosine tapers, exponential tapers and linear ridge taper transitions it was decided to design a linear taper with a theoretical VSWR performance of 1.05 over the full Q-band. The average measured r.f. transmission loss and VSWR of a back to back waveguide 22 linear ridge transition to a 50 ohm linear ridge waveguide section, in the frequency band 26 to 40 GHz, were 0.5 dB and 1.08 respectively. A portion of the full ridged waveguide section could be replaced by an enclosure containing the microstrip test circuits. The enclosure being designed to suppress box resonances in the frequency band of interest. The r.f. loss in the frequency range of 26-33 GHz of two waveguide to microstrip transitions and a microstrip line containing two beam-lead capacitors for d.c. blocks, fabricated on quartz was approximately 0.8 dB. Circuits using a beak pressure contact to make continuity between the waveguide transition and microstrip line, resulted in slight crazing of the

substrate surface causing significant increase in loss and VSWR of the transition. Transitions using gold tape to make connection to the microstrip line gave a more reproducible r.f. performance.

TECHNOLOGY

For high frequency applications particular care has to be taken in the manufacture and the assembly operations of the microstrip circuit to ensure minimum r.f. loss characteristics. The transmission loss of the microstrip circuit on quartz (fused silica) was found to deteriorate after thermal compression bonding. On examination of the microstrip line it was found that it had started to tear from the fused silica substrate, leaving a tear channel in the substrate. The tearing was caused by the difference in thermal expansion coefficients between the gold line and the substrate material. To eliminate this problem a crystalline-cut quartz was chosen with similar thermal expansion coefficient to gold. The substrates were mounted on thermally compatible substrate carriers.

APPLICATIONS

Figure 5 shows a photograph of the high frequency test jig, with waveguide 22 transitions, quartz substrate and mounted GaAs FET device, the d.c. inputs to the device being supplied via a bias filter. The r.f. isolation through the jig was greater than -40 dB. It was found that at high frequencies with device gains of 5.0 dB and second-stage noise figures of the order of 10 dB, the accuracy of deriving chip noise figures becomes very dependent upon the accuracy with which circuit losses can be measured. For this reason substrate noise figures were measured, i.e. incorporating microstrip and bias network losses. The substrate noise figures along with an average loss figure for the microstrip circuit were used to derive an average chip noise figure of 3.9 + 0.2 dB for the frequency band 29.5 + 2.5 GHz (9,10). This test jig and microstrip analysis allowed the S_{11} and S_{22} parameters of the FET chip to be measured. These compared very favourably with the extrapolation of S-parameters from low frequency measurements (<18 GHz).

CONCLUSIONS

The design and measurement techniques presented have allowed the characterisation of FETs in Q-band, and the preliminary design of single-stage Q-band amplifier modules.

ACKNOWLEDGEMENTS

The authors would like to thank Dr. T. Edwards and Mr. E. England of the Royal Military College, Shrivenham for discussion and a microstrip computer programme using the Itoh and Mittra routine, and Drs. B. Davies and D. Mirshekar-Syankal of University College, London for their microstrip analysis computer programmes.

This work has been carried out with the support of Procurement Executive, Ministry of Defence, sponsored by DCVD, and has been performed in part under the sponsorship and technical direction of the European Space Agency (ESA).

REFERENCES

1. Spectral domain approach for calculating the dispersion characteristics of microstrip lines', T. Itoh and R. Mittra, IEEE Trans. MTT, July 1973.

2. 'Microstrip dispersion model' W. Getsinger, IEEE Trans. MTT January 1973.

3. '2-18 GHz dispersion measurements on 10-100 microstrip lines on sapphire' T. Edwards and R. Owens, IEEE MTT August 1976.

4. 'Losses in microstrip', R.D. Pucel, D.J. Masse and C.P. Hartwing, IEEE 16, June 1968 and Correction to Losses in microstrip, Dec. 1968.

5. 'The technology of microwave integrated circuits' H. Sobel and M. Caylton Advances in Microwaves, Chapter 1, Vol. 8, 1974.

6. 'Dielectric loss in integrated microwave circuits' M.V. Schneider, Bell System, Tech. J. 48, No. 7, Sept. 1969.

7. Microstrip Handbook. G.O. Hammerstead and F. Bekkadel.

8. 'A 31 GHz monolithic GaAs Mixer/preamplifier circuit for receiver applications' A. Chu, W. Courtney and R. Sudbury, IEEE Trans. Ed, Vol. ED-28, Nos. 2, Feb. 1981.

9. 'Extended frequency range GaAs MESFETs using 0.3μm gate length, J. Arnold, R.S. Butlin, EMC 1981 Amsterdam.

10. '26-40 GHz Q-band FETs' C. Oxley et al, IEDM Dec. 1981.

203

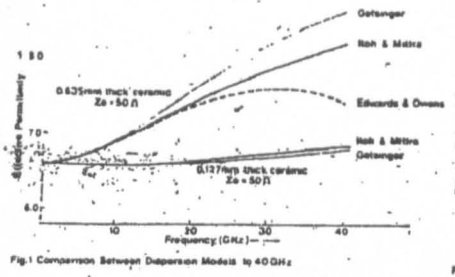


Fig.1 Comparison Between Dispersion Models to 40 GHz

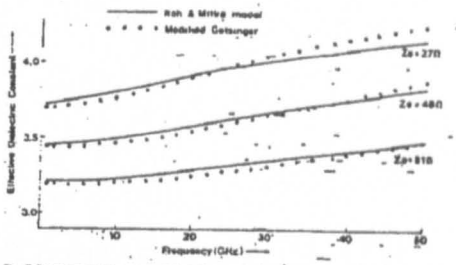


Fig. 2 Comparison Between the Itoh & Mehra Model & the Modified Getsinger Model for Microstrip Lines on Quartz Substrates

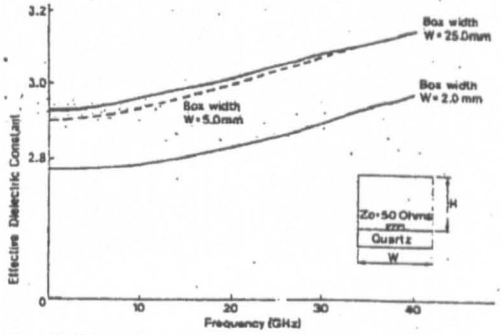


Fig. 3 The Effect of Changing the Enclosure Width

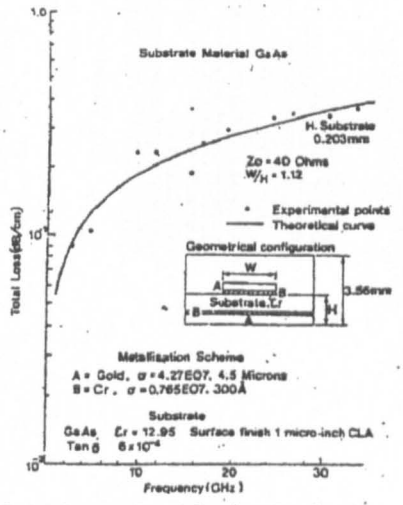


Fig. 4 A Comparison Between Experimental Data (Courtney IEEE Trans Ed. Feb 1981) and Theoretical Plot Produce by the Computer Programme

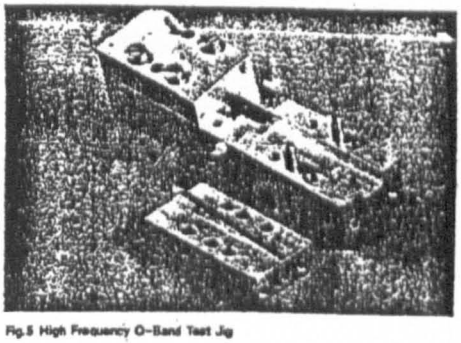


Fig.5 High Frequency C-Band Test Jig

294

Q-BAND (25–40 GHz) GaAs FETs

C.H. Oxley, A.H. Peake, R.H. Bennett, J. Arnold and R.S. Butlin

Plessey Research (Caswell) Ltd., Allen Clark Research Centre,
Caswell, Towcester, Northants., NN12 8EQ, United Kingdom

ABSTRACT

Gallium arsenide FETs demonstrating maximum gains of 4 dB at 40 GHz have been fabricated using combined photolithographic and electron beam lithographic techniques.

The device structure has been optimised for high frequency performance. An equivalent circuit model has been derived from low frequency S-parameter data demonstrating good agreement with measured high frequency results. Device noise figures of 1.2 and 2.1 dB have been demonstrated at 12 GHz and 18 GHz respectively. At 27 GHz a substrate noise figure (i.e. including substrate losses) of 3.6 dB with 6.0 dB associated gain has been obtained. Low temperature (-77°K) noise figures of 0.3dB have been obtained at 14 GHz.

INTRODUCTION

The Gallium Arsenide (GaAs) low noise MESFET amplifiers are now becoming an accepted component of radar, communication and various electronic warfare systems. With the event of future systems requiring lower noise front-ends and higher frequency operation, the GaAs MESFET is being continually developed to meet these requirements.

This paper will describe the design and fabrication of electron beam (EB) devices which have exhibited noise figures of 1.2, 1.6 and 2.1 dB at 12, 14 and 18 GHz respectively, and substrate noise figures (i.e. including substrate losses) of 3.6 dB at 27.0 GHz.

DEVICE DESIGN AND TECHNOLOGY

To realise a high frequency low noise FET the gate length has to be reduced and the device parasitic minimised. The parasitics which most affect the n.f. performance are source resistance, gate metallisation loss and source inductance. The noise theory of Fukui (1) was used to examine the effects of device structure (2) and fabrication technology (2) on the device noise performance to 40 GHz.

The device high frequency gain is significantly dependent upon the magnitude of the source inductance, and unlike the gate and drain inductances it cannot be tuned out by the input and output matching networks. Although a reduction in the source to ground inductance may be obtained by using a multi-bond wire configuration there is a significant mutual inductive effect between the closely-placed bond-wires, thereby preventing the full reduction in inductance being realised. Figure 1 shows a photo of a 0.3 micron gate-length orthogonal single cell device design (CI-structure) which incorporates trapezium shaped source pads for low inductive wide tape-bonding. The source pads appeared not to contribute significantly to the device parasitics. The mesa was also designed to be outside of the source pad outline to provide a planar bonding area. The device unit gate-width is 50.0 microns which offers matchable device impedances. The gate metallisation was widened over the mesa-edge to avoid current crowding. Careful consideration was also given to the gate bonding pads to minimise parasitics, especially capacitance, since the latter could dominate the capacitance of the active region.

The device was mounted in a well seated on a ridge (Figure 2), allowing short tape source bonds to ground to be used. The estimated source inductance with 0.1ℓ mm wide gold-tape was <0.04nH compared with <0.07nH for a multi-bond wire configuration.

An alternative structure using angled gates has also been fabricated (Figure 3). The angled structure helps to minimising the feedback capacitance, and offers a reduction in undercutting during the formation of the gate channel, therefore further reducing the source-gate, gate-drain resistance. The figure also shows the chip identification numbering system for automatic d.c. probing.

The high frequency FET active region was doped to approximately 2.0×10^{17} atoms/cc. In/Ge/Au ohmic source and drain contacts were used with aluminium Schottky gates. The fabrication processes have been covered in previously published papers (2,3) and consisted of a combined photolithographic and electron beam lithographic technology.

DEVICE CHARACTERISATION

Device S-parameters were measured to 18 GHz using a HP automatic network analyser, with slotted line measurements for high frequency characterisation. For the S-parameter measurements up to 18 GHz the device was mounted on a post which was inserted through an alumina substrate. The device was bonded to 50 ohm lines on the substrate and

ALL MATERIAL IN THIS SPACE WILL BE OUTLINED

connection to the equipment was made via SMA connectors while a waveguide/microstrip circuit to be described was used for the high frequency measurements. The chip data was obtained by using microstrip de-embedding techniques. A number of chips were measured and a simple unilateral model from the averaged data was derived. The reverse isolation characteristics were exceptionally low with S_{12} of the order of 0.03 at 18 GHz.

The unilateral model along with d.c. chip measurements of intrinsic resistance (R_i), source resistance (R_s) and the drain resistance (R_d) led to the derivation of a full equivalent circuit model (Fig. 4) for the 0.3 micron orthogonal structure. Good agreement between experiment and theory was obtained for the S_{11}, S_{22} and S_{21}, but although similar magnitudes for the S_{12} could be obtained, there were large discrepancies in phase angle. Using the model the S-parameters for the 0.3 microns orthogonal structure were extended to 40 GHz. A few preliminary S_{11} measurements were made at high frequencies, and reasonable agreement was found between experiment and theory.

RF PERFORMANCE

Noise and gain measurements to 18 GHz have indicated significant improvements over the 0.5 micron gate-length device. The measured noise figure of the 0.3 micron device at 12, 14 and 18 GHz was 1.2, 1.5 and 2.1 dB, and the corresponding associated gains were 12.6, 11.0 and 9.0 dB, while the measured noise figure of a 0.5 micron device at the same frequencies were 1.9, 2.2 and 3.0 dB. Further improvements in the noise figure of the 0.3 micron device at 14 GHz have been realised by cooling the device. At temperatures of -40°C which can be readily obtained by thermo-electric cooling the device, the measured noise figure was improved by approximately 50%, while at an ambient temperature of 77°K the device noise temperature was 23.0°K (0.33 dB) with 11.6 dB associated gain.

High frequency r.f. results have been measured (26-40 GHz) for both the 0.3 micron gate length orthogonal and angled structure. A microstrip circuit media was favoured after extensive computer analysis. A number of microwave substrates were analysed, using the ITOH and MITTRA model (4) and taking into account dielectric losses, conduction losses (including multi-metal systems) and losses due to surface finish. A polished quartz substrate 0.381 mm thick was finally chosen as it offered low loss at high frequencies (for example a 50 ohm line had a computed loss of 0.07 dB/cm at 30 GHz), and a line-width sufficiently wide to ease the design of transitions. To realise a high-frequency mode free transition a waveguide E2 linearly tapered ridge approximately three wavelengths in length at 40 GHz was designed (5,6). The connection between the taper and the microstrip line was made by 0.38 mm wide gold tape. RF measurements of the back to back waveguide transition from 26 to 40 GHz, have shown a loss of approximately 0.5 dB and a maximum VSWR of 1.15 across Q-band. Figure 5 shows a complete high frequency test-jig. The bias to the device was supplied via a stitch-bond filter, and the d.c. isolation was obtained by bond lead capacitance. The measured r.f. loss of the bond transitions, 10 mm of microstrip line, and d.c. blocks was of the order of 0.8 dB in the frequency range 26-32 GHz. External tuning of the device for gain and noise performance was achieved using waveguide E/H tuners. Fig. 6 shows the measured MAG at 1 dB of the 0.3 micron orthogonal and angled device structures, to 40 GHz. The results show reasonable agreement with the MAG values predicted using the equivalent circuit model.

Noise figure measurements of the 0.3 micron orthogonal structure were made to frequencies approaching 33 GHz. At these frequencies, with device gains in the region of 5 dB and with second-stage noise figures of up to 10 dB, the accuracy of deriving chip noise figures becomes very dependent upon the accuracy with which circuit losses can be measured. For this reason substrate noise figures are quoted, i.e. incorporating microstrip and bias network losses. Figure 7 shows substrate noise and associated gain measurements for the 0.3 micron devices between 26.6 to 32.6 GHz. The substrate noise figures along with an average loss figure for the microstrip circuit, were used to derive an average chip noise figure for the frequency band 29.6 ± 2.5 GHz. This value was plotted (Figure 8) along with the low frequency noise measurements for 0.3 micron devices from the same batch of chips (Curve A). The figure also includes the best low frequency 0.3 micron device noise figures measured to date (Curve B). Both plots are compared with the theoretical noise curve.

Reliability tests have shown that 0.3 micron device length devices have a predicted mean time to failure of 10^7 hours at room temperature, and 10^6 hours at 70°C. Burnout tests established that the devices could withstand in excess of 0.5 watt CW.

CONCLUSIONS

The feasibility of using 0.3 micron gate length FETs for Q-band (26-40 GHz) operation has been demonstrated. At 27.0 GHz substrate noise figures of 2.5 dB and associated gains of 6.0 dB have been recorded, while MAG gains as high as 4.0 dB at 40.0 GHz have been measured. Improvements of 50% in noise figure in J-band have been observed for devices which are cooled to -40°C, these could offer a serious competitor to the parametric amplifier. The 0.3 micron orthogonal device structures have been shown to have a MTTF of 10^6 hours at 70°C.

ACKNOWLEDGEMENTS

This work has been carried out with the support of Procurement Executive, Ministry of Defence, sponsored by DCVD, and has been performed in part under the sponsorship and technical direction of the International Telecommunications Satellite Organisation (INTELSAT). Any views expressed are not necessarily those of INTELSAT. The authors would like to thank in particular their colleagues responsible for the bonding and assembly of the microstrip test-circuits.

Gain at 40GHz 7db - 8db
NF at 32Gh 3.2db 5.5 - 6db

REFERENCES

(1) H. Fukui et al, ELECTRON LETT., 11 (12), p.309, 1976.

(2) R.S. Butlin et al, "J-Band Performance of 300 nm Gate-length GaAs FETs", PROC IEDM, Washington, 1978.

(3) R.S. Butlin et al, "200 nanometre Gate Length FETs" Cornell Electrical Engineering Conf., Proc. Vol. 6, 1977.

(4) T. Itoh and Mittra, "Special-Domain Approach for Calculating the Dispersion Characteristics of Microstrip Lines" IEEE, MTT, July 1973.

(5) K. Matsumaru, "Reflection Coefficient of E-Plane Tapered Waveguide" IRE Trans. MTT, April 1958.

(6) W. Hoefer, "Quickly Now, Where does Waveguide Cut-off Occur", MICROWAVES, Dec. 1979.

Figure 1

CI, ORTHOGONAL 0·3 MICRON DEVICE

Figure 2

CI DEVICE BONDED INTO MICROSTRIP CIRCUIT

Figure 3

0·3 MICRON ANGLED GEOMETRY

Figure 4

LOW NOISE BIAS MODEL OF E-B FET

ALL MATERIAL IN THIS SPACE WILL BE DELETED

Figure 5 HIGH FREQUENCY TEST-JIG

Figure 6 MAXIMUM AVAILABLE GAIN (MAG) OF 0.3 MICRON EBT's

Figure 7 SUBSTRATE NOISE FIGURE AND ASSOCIATED GAIN

Figure 8 NOISE FIGURE PERFORMANCE OF 0.3 MICRON GATE-LENGTH DEVICES

This implanter has been used to produce SIMOX wafers, which are then incorporated into MOSFETs. Such MOSFETs are found to have excellent characteristics. Thus, the newly developed 100 mA-class high-current oxygen implanter has proved to be capable of contributing to the advancement of SIMOX technology. It will also contribute to expediting the practical application of SIMOX technology.

Acknowledgment: The authors would like to thank M. Kondo, N. Ohwada and T. Sakai for their guidance and encouragement.

K. IZUMI
Y. OMURA
S. NAKASHIMA
Atsugi Laboratories
NTT Electrical Communications Laboratories
3-1, Morinosato Wakamiya
Atsugi-shi 243-01, Japan

28th May 1986

References

1 IZUMI, K., DOKEN, M., and ARIYOSHI, H.: 'CMOS devices fabricated on buried SiO_2 layers formed by oxygen implantation into silicon', *Electron. Lett.*, 1978, **14**, pp. 593–594

2 PINIZZOTTO, R. F., VAANDRAGER, B. L., MATTESON, S., LAM, H. W., MALHI, S. D. S., HAMDI, A. H., and MCDANIEL, F. D.: 'The top silicon layer of SOI formed by oxygen ion implantation', *IEEE Trans.*, 1983, **NS-30**, pp. 1718–1723

3 HEMMENT, P. L. F., MAYDELL-ONDRUSZ, E., STEPHENS, K. G., ARROWSMITH, R. P., GLACCUM, A. E., KILNER, J. A., WILSON, M. C., and BOOKER, G. R.: 'Oxygen and defect distributions in silicon on insulator structures formed by high dose O^+ implantation into silicon'. Proceedings of international ion engineering congress—ISIAT'83 & IPAT'83, Kyoto, pp. 1855–1860

NEW WIDEBAND GaAs TRAVELLING-WAVE DEVICE: LINEAR GATE TRANSISTOR

Indexing terms: Microwave devices and components, Travelling-wave devices

A new device called the linear gate transistor (LGT) is described which promises in excess of 20 GHz flat-band performance in a single compact structure. The LGT is designed and modelled using a unique software package developed for all travelling-wave structures. Results from a prototype LGT are reported.

Introduction: In a previous publication[1] the authors reported details of a travelling-wave FET (TWF) and described in detail modelling software essential to its design and optimisation. Subsequently this model was developed by us to encompass both the TWF and th so-called travelling-wave amplifier (TWA) reported by the Raytheon Group,[2] amongst others. The new model[3] extended the novel coupled active transmission-line method to include meandered electrodes. Using this extended model the two device variants were compared and their respective advantages and disadvantages enumerated.[3] In brief, the TWF displays a growing wave, whereas the TMA enjoys a more conventional gain mechanism. As a result the TWA is limited in the number of active devices it can use in series whereas the TWF growing wave continues to grow through many active units. However, the TWA displays better gain per unit total gate width and a better impedance. It also can be 'single-end-fed' unlike the TWF, which required a balanced input and output.

With the help of the unified model a new device the linear gate transistor (LGT) was invented[4] which combines the advantages of both the TWA and TWF.

Fig. 1 shows a photograph of a small prototype LGT device. In essence the LGT is a single FET device like the TWF with a wide gate. In contrast to the TWF the drain is meandered between active units to provide phase-matching of the travelling waves (the TWF used overlay capacitors) similar to the TWA. Unlike the TWA the single linear gate allows the drain line to approach at the active sections and establish inductive coupling. This inductive coupling has been shown by us[1] to be essential for the production of a growing wave. When the LGT is simulated using the extended model a growing wave is observed but with the added advantage of higher gain and improved impedance. These latter effects are due to the meandered drain line introducing inductive rather than capacitive loading.[3] The growing wave in the LGT enables as many as ten active units to be used in a single compact device. The LGT operation is dominated by conventional mode swopping (see Reference 3) like the TWA near the input end and at low frequency and the growing wave phenomena further down the gate and at higher frequency. As such the growing wave does not have to be matched at the outset, and so the device is single-end-fed on the gate line only (a major advantage).

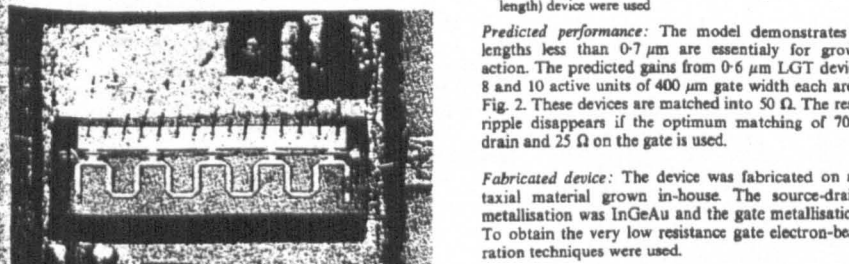


Fig. 1 *Photograph of a 5-unit LGT device*
2 mm total active gate width

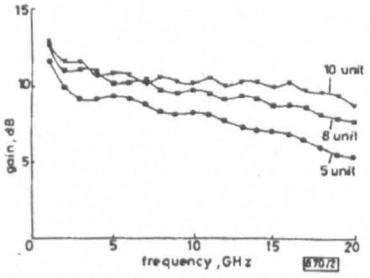


Fig. 2 *Modelled performance of optimised LGT devices with 5, 8 and 10 units of 400 μm gate width*
Intrinsic parameters scaled from Plessey GAT6 (~0·7 μm gate length) device were used

Predicted performance: The model demonstrates that gate lengths less than 0·7 μm are essentialy for growing wave action. The predicted gains from 0·6 μm LGT devices with 5, 8 and 10 active units of 400 μm gate width each are shown in Fig. 2. These devices are matched into 50 Ω. The residual gain ripple disappears if the optimum matching of 70 Ω on the drain and 25 Ω on the gate is used.

Fabricated device: The device was fabricated on *n*-type epitaxial material grown in-house. The source-drain contact metallisation was InGeAu and the gate metallisation TiPtAu. To obtain the very low resistance gate electron-beam evaporation techniques were used.

Results: Fig. 3 shows the measured performance of the prototype 5-unit device together with the modelled results using the low frequency and DC measurements to generate the equivalent circuit. It is seen that the agreement with the predicted results is very good. The performance is below optimum because the resultant FET structure fell short of the optimum

in terms of g_m, gate resistance and gate capacitance, although the 0·6 μm gate length was achieved.

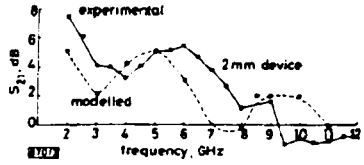


Fig. 3 *Measured and modelled S21 for a prototype 5-unit LGT module*
Intrinsic parameters were extracted from low-frequency and DC measurements and were not optimum for the design

Noise measurements: The noise figure of the device was measured over a wide band using the Eaton noise gain analyser. Without any tuning the module noise and gain performance are shown in Fig. 4, and from the measurement it can be seen that a relatively flat noise performance is obtained on around 6·5 dB. It is also interesting to note that under the same bias conditions the module gave a −1 dB output power of approaching 100 mW with a third-order intermodulation product of approximately −35 dB.

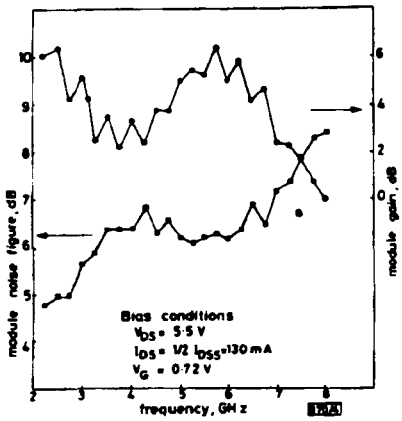


Fig. 4 *Noise figure and gain for an LGT module as a function of frequency*
$I_{DS} = \frac{1}{2} I_{DSS}$

Conclusion: A new device, the linear gate transistor (LGT), has been described which combines the advantages of TWF and TWA structures and shows a true growing wave. Predicted performance suggests gains in excess of 9 dB over a 20 GHz bandwidth from a single compact device which does not require cascading.

Measured results show encouraging agreement with a new extended computer model.

Acknowledgment: Part of this work was carried out with the support of the Procurement Executive, Ministry of Defence (Directorate of Components, Valves and Devices) sponsored from the Royal Signals and Radar Establishment).

A. J. HOLDEN
I. DAVIES
P. MEDHURST
C. H. OXLEY

Allen Clark Research Centre
Plessey Research (Caswell) Ltd.
Caswell, Towcester, Northants NN12 8EQ, United Kingdom

28th May 1986

References

1 HOLDEN, A. J., DANIEL, D. R., DAVIES, I., OXLEY, C. H., and REES, H. D.: 'Gallium arsenide travelling wave field effect transistors', *IEEE Trans.*, 1985, ED-32, pp. 61–66

2 AYASLI, Y., REYNOLDS, L. D., VORHAUS, J. L., and HANES, L.: 'M... lithic 2–20 GHz GaAs travelling-wave amplifier', *Electron. L...* 1982, 18, pp. 596–598

3 HOLDEN, A. J., and OXLEY, C. H.: 'Computer modelling of trav... wave transistors'. Proceedings of international conference on ... lation of semiconductor devices and processes, Swansea 1984, ... 319–329 (Pineridge Press, Swansea, UK, 1984)

4 British patent GB2156152A

ACCURATE LOOP LENGTH DETERMINATION IN FIBRE-OPTIC SENSOR AND SIGNAL PROCESSORS

Indexing terms: Optics, Fibre optics, Optical sensors, Opti... processing

A technique is demonstrated for the accurate determinat... of differential propagation delays in fibre-optic circuits co... monly found in sensing and signal processing arrays, utilisi... the high-order frequency filtering characteristics of these ... cuits. Relative time delays for two interferometers can ... easily compared to within less than 10 ppm.

Fibre-optic coils used as delay lines are quite common the... days in both interferometric fibre-optic sensors,[1] and in fibr... optic signal processors.[2] Two basic forms of fibre circui... using such delay lines are the feed-forward (forward-flo... Mach-Zehnder circuit (Fig. 1*a*) and the feed-backwar... (backward-flow) recirculating loop (Fig. 1*b*). A delay line o... may be inserted into an interferometer to produce a lar... difference in the propagation delays τ_1 and τ_2 (Fig. 1*a*) or in... a recirculating delay line to give a large value to the roun... trip delay τ (Fig. 1*b*). Very often there is a need for an accura... determination of the relative propagation delays in such ci... cuits. In sensor arrys, uncompensated imbalances in th... various loop lengths require the use of excessively long cohe... ence sources,[3] and/or introduce phase-induced intensit... noise.[4] Also, the performance of complicated fibre-optic lattic... filters depends critically on the tolerances of the delay li... lengths.[5] These tolerances may reach 1 mm in 100 ... (10 ppm). In this letter we analyse a measurement techniqu... for τ which makes use of the filtering properties of these ci... cuits, when driven by radio frequency (RF)-modulated inco... herent sources. In particular, we show that, as far as R... leakage permits, going to higher frequencies monotonical... increases the resolution of the measurement.

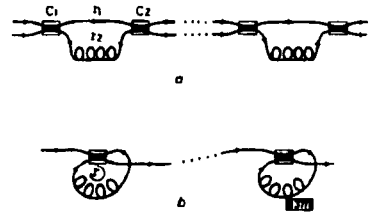


Fig. 1 *The two basic circuits used in fibre sensors and signal process...*
a Feed-forward circuit; τ_1 and τ_2 are delays along the tw... branches and $\tau = \tau_1 - \tau_2$ is the differential delay. C_1 and C_2 ... two couplers
b Recirculating, or feed-backward, loop; τ is the loop delay

Consider the feed-forward circuit of Fig. 1*a*. When drive... by an RF intensity-modulated optical source, whose cohere... ence length is much shorter than the differential delay τ = ... $\tau_1 - \tau_2$, the transfer function $T(f)$ is the sum of the two inte... sity phasors from the two branches of the circuit:

$$T(f) = A_1 \exp[(2\pi j f \tau_1)] + A_2 \exp[(2\pi j f \tau_2)] \quad (1)$$
$$= M(f) \exp\{[j\theta(f)]\}$$

Gallium Arsenide Traveling-Wave Field-Effect Transistors

ANTHONY J. HOLDEN, DAVID R. DANIEL, IAN DAVIES, CHRISTOPHER H. OXLEY, AND H. D. REES

Abstract—The design, modeling, and fabrication of a GaAs traveling-wave field-effect transistor (TWF) is reported. The TWF described is a device with a single continuous 1-μm-long gate and a total width of 3 mm which shows flat band gain from 1 to 10 GHz with the potential of much wider band performance (1–40 GHz) and high gains. An advanced theoretical model is presented which performs a full coupled transmission line modal analysis for three lines (source gate and drain) using *ab-initio* calculations of interelectrode capacitance and inductance matrices. Good agreement is demonstrated between theory and experiment for frequency gain response measurements using balanced feed circuits.

I. Introduction

ALTHOUGH the concept of traveling-wave operation is not new [1], [2], the realization of such action in a single semiconductor device is reported here, we believe, for the first time. Traveling-wave amplifiers consisting of a distributed network of discrete devices have recently been reported [3]–[6], but the device to be described in this paper is a single field-effect transistor (FET) with a very wide gate of 1 μm in length which exhibits traveling-wave action along a virtually continuous active width, the waves being balanced by periodically positioned overlay capacitors. The parasitic resistance in such a wide gate is overcome by using a T-shaped gate cross section.

We present a detailed mathematical model of the device including, for the first time, *ab-initio* calculations of the mutual inductance and capacitance of the source, gate, and drain electrodes and a full three-coupled transmission line modal analysis with the active admittance modeled by a distributed intrinsic circuit. Devices of both 1.2-mm and 3-mm gate width (Fig. 1) have been fabricated and measured and the results reported show excellent agreement with the theoretical predictions.

II. Traveling-Wave Operation

Traveling-wave operation has the advantage of wider bandwidth operation over conventional FET's coming from the low dispersion in the device which is due mainly to the transmission lines. Parasitics in the transistor make the lines less than ideal, but in theory flat band performance from 1 to 30 GHz and beyond should be possible. Traveling-wave devices work as many parallel amplifier stages offering distinct advantages over FET's in series. The "distributed" or "traveling-wave" amplifiers (TWA) reported in the past operate in a fundamentally different way to the device described here and are limited in the total number of device "units" that they can distribute (without, that is, "cascading" independent TWA's as in [5]). The traveling-wave FET (TWF) described in this paper makes use of an exponentially growing wave mode which continues to grow across the whole width of the device. Provided that this particular mode can be successfully matched in and out of the device, the amount of available gain is simply dependent on the total device width. Widths of 10 mm or more can be envisaged. A detailed comparison between TWA and TWF devices may be found in [7].

The basic theory of traveling-wave devices has been developed in the past both for distributed amplifiers (TWA's) [3] and for TWF's of the type described in this paper [9], [10] although the theory developed here is the first to take all three coupled lines together with the full intrinsic circuit into account. In all theories the need to balance waves on the gate and drain lines is demonstrated. This is due to the large depletion capacitance on the gate line compared with the capacitance on the drain line (see Section III). The method used to compensate this extra capacitance is what distinguishes the TWA devices from the TWF described here. In the TWA the drain line is made longer than the gate line between active elements whereas in the TWF compensation is effected by loading additional capacitance onto the drain line. This capacitance has a dramatic effect on the eigenmodes of the system and produces the strong growing mode as discussed in Section III. In the TWA the meander has a very different effect on the modes producing a more conventional gain characteristic [7].

III. Theoretical Analysis

A schematic representation of a traveling-wave field-effect transistor (TWF) is shown in Fig. 2. The device consists of three coupled electrodes fabricated on a thin layer of gallium arsenide (GaAs), supported by a semi-insulating GaAs substrate. The three electrodes are in the same sense as a conventional FET, i.e., drain, gate, and source.

The analysis of this structure is very complex and to the authors' knowledge has not been tackled rigorously to date. Existing theories [6], [9] treat the gate and drain as separate transmission lines coupled only by the transconductance; the full "three-line" mode structure is not analyzed.

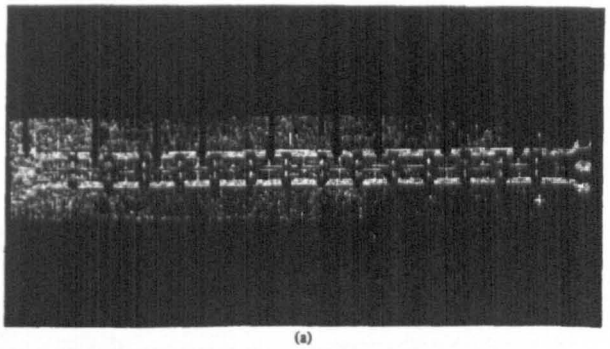
Manuscript received May 31, 1984; revised August 27, 1984. Part of this work was supported by the Procurement Executive, Ministry of Defence, sponsored by DCVD.

A. J. Holden, I. Davies, and C. H. Oxley are with Plessey Research (Caswell) Ltd., Caswell, Towcester, Northamptonshire, England.

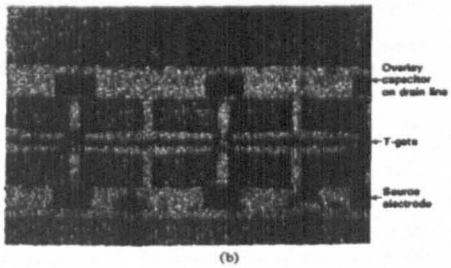
D. R. Daniel was with Plessey Research (Caswell) Ltd., Caswell, Towcester, Northamptonshire, England. He is now with STC Components, Paignton, Devon, England.

H. D. Rees is with R.S.R.E., Malvern, Worcestershire, England.

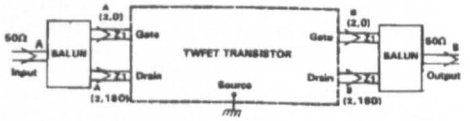
0018-9383/84/0100-0061$01.00 © 1984 IEEE



(a)



(b)



(c)

Fig. 1. (a) Photograph of a fabricated traveling-wave FET with a total gate width of 3.3 mm (3 mm active). (b) Detail of TWF showing electrode arrangement. (c) Feed arrangement, showing balun circuits producing a 180° phase split between gate and drain and transforming the impedance to 20 Ω on each line.

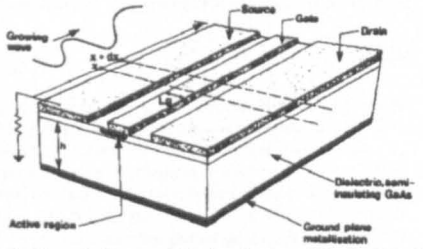


Fig. 2. Schematic diagram of the traveling-wave FET geometry showing the coupled microstrip lines and the central "active" region.

In this work the structure is analyzed by separating the calculation into two parts. 1) The device electrodes are considered as a multicoupled microstrip transmission line problem. 2) The active region of the FET is analyzed by treating the equivalent circuit of the FET as distributed along the device width.

A. Transmission Line Geometrical Inductance and Capacitance Matrices

To solve the coupled transmission line problem, the geometrical inductance and capacitance matrices for the passive conductors are first calculated. Following the work of Silvester [11] we apply a Green function method to calculate the capacitance per unit length in this multiconductor system. The object is to numerically evaluate a charge matrix in which the components K_{mn} relate the total charge per unit length on conductor $m(Q_m)$ and the potential on conductor $n(V_n)$ by the matrix equation

$$\begin{pmatrix} Q_1 \\ Q_2 \\ Q_3 \end{pmatrix} = (K) \begin{pmatrix} V_1 \\ V_2 \\ V_3 \end{pmatrix}. \tag{1}$$

The capacitance matrix C_{mn} can then be obtained from K_{mn} by reference to the circuit admittances A_{mn} in Fig. 3 where

$$A_{mn} = j\omega C_{mn}. \tag{2}$$

Here ω is the angular frequency and $j = \sqrt{-1}$. We obtain

$$C_{nn} = K_{nn} + \sum_{m \neq n} - K_{mn}. \tag{3}$$

Off-diagonal capacitances are simply

$$C_{nm} = -K_{nm}. \tag{4}$$

To obtain the charge matrix K we divide the conductors into strips and then evaluate the potential on one strip due to a

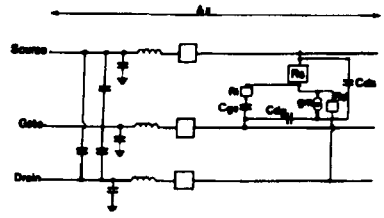


Fig. 3. An element "Δx" of the equivalent circuit showing the geometrical capacitance and inductance contributions and the "active" equivalent circuit. Some of the circuit elements have been omitted to aid clarity.

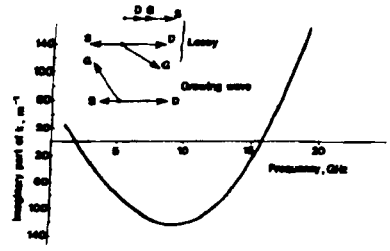


Fig. 4. Phasor diagrams for the voltages in each of the three traveling-wave modes and the imaginary part of the propagation constant k for the growing wave showing substantial negative values. These results are for the 1-μm (GAT4) parameters but the qualitative results apply to a range of equivalent circuit parameters.

single line charge on another strip, taking care to include all the image charges produced by the "hall of mirrors" effect of the ground plane and dielectric-free space interface.

The resultant Green function is integrated in the manner of Silvester over a general charge distribution on all the conductors and a matrix equation results

$$V = Pq. \tag{5}$$

Here V is a column vector of voltages on all the strips and q the corresponding column vector of strip charges. Inverting (5) yields the charge configuration for a particular voltage configuration. Summing charge over particular conductors yields the charge matrix K. By repeating the calculation with the substrate dielectric equal to the free-space value, the inductance matrix may be obtained within the TEM approximation by solving for the eigenmodes and using the fact that the mode velocities must equal the velocity of light in free space (W_L). This is a generalization of the standard microstrip inductance calculation (Silvester [11]) and yields the inductance matrix

$$L = \frac{1}{W_L^2} K^{-1} \tag{6}$$

enabling the inductance to be calculated from the charge matrix for $\epsilon = \epsilon_0$. This inductance matrix remains valid when the substrate is returned because the GaAs is nonmagnetic.

The computer model calculates the Green function, inverts the matrix, and evaluates capacitance and inductance matrices for N lines. The routine has been used for N up to 12. By calculating the transmission properties (as described in the Appendix) for passive microstrip lines, good agreement has been found with other standard routines for one- and two-line systems and agreement with experiments on coupling between two and three passive microstrip lines has been achieved [8]. As is usual for this type of calculation the method is most accurate for long narrow systems. Line end effects, however, can be taken into account by the modeling of reactive terminations.

B. Active Admittance

The key to modeling the TWF is the inclusion of the active nature beneath the gate. A full field analysis of the carrier transport within a waveguide environment, although intriguing, is beyond the scope of the present treatment. Instead we formulate quasi-TEM solutions from an equivalent distributed circuit for the transmission lines complemented by a distributed form of the FET equivalent circuit [12] (see Fig. 3).

Extra resistance incurred from source to gate and gate to drain due to the enlarged structure, additional capacitance associated with the T cross section gate, and extra overlay capacitance between source and drain electrodes have been included.

The additional "active" elements can be thought of as an active admittance matrix which is added to the more usual passive admittance matrix found for coupled transmission lines. The derivation of both these admittance matrices is outlined in the Appendix. The values taken for the intrinsic elements are obtained from dc and low-frequency S-parameter measurements on TWF devices or scaled from conventional devices having similar gate lengths and material properties.

C. Transmission Line Modes

Given the complete impedance and admittance matrices Z and Y, the Appendix shows that the eigenvalue equation takes the form of (A5). Y, however, no contains the active elements and is in general nonsymmetric. The equation is solved numerically using a standard library routine. For the TWF it is a 3 X 3 problem, but higher order systems can be tackled. As the system contains resistance and reactance the equations are also complex, leading to amplitude and phase for voltage and current and complex propagation constants. For the TWF there are 6 modes (three forward traveling and three reverse) consisting of three independent eigenvectors with three eigenvalues. (Each eigenvalue can be positive or negative.)

The eigenvectors take the form of (A5b) and Fig. 4 shows the eigenvectors for a TWF with additional source drain capacitance set equal to the distributed depletion capacitance C_{dep}. The first two modes are lossy; they have a positive imaginary k in (A5b) just as in conventional transmission lines. Mode 3, however, has a negative imaginary propagation constant over some useful bandwidth, and so this mode will *grow* as it travels along the device. Essential to the appearance of this growing mode is the dominance of the inductive reactance over the line resistance. This is achieved by spacing the source and drain electrodes over 100 μm apart as seen in Fig. 1.

Without the additional source drain overlay all three modes are found to be lossy, and the reason for the change can be understood if we consider the simple case of decoupled gate and drain transmission lines. The dominant capacitance is the depletion capacitance C_{dep} which appears on the gate line. Waves on the gate will thus be slower than waves on the drain. In order to drive the transistor throughout its width the drain voltage must stay in step (or, more precisely, 180° out of step) with the gate voltage, and so extra drain source capacitance is added of similar size to C_{dep} to achieve balance and allow a wave to grow. The fact that the mode grows efficiently is due to the feed-back effect of the inductance between drain and gate which compensates for the high loss of the gate line.

IV. Feeding the Transistor

In order to operate the device with the correct growing wave mode and to avoid exciting the other lossy modes, it is necessary to feed with the appropriate mode form and ensure good input and output matching for the mode in question.

Examination of the growing mode voltage vectors (Fig. 4) reveals that the gate and drain voltages have roughly equal amplitude but are almost 180° out of phase. The source voltage is comparatively small. An acceptable match to this mode can be achieved by balance feeding the signal onto the gate and drain lines and outputting into a similarly balanced circuit. The source line can be conveniently earthed.

To establish the matching impedances, the characteristic impedances of the active transmission line must be calculated. If we assume that only one mode is propagating, a set of characteristic impedances for that mode can be derived from the calculated currents and voltages. We define R_{io} as the characteristic impedance between the ith line and ground calculated for the one mode. In the TWF, R_{io} has only a small reactive part (the voltage and current vectors are nearly in phase) enabling wide bandwidth matching. Although there is some slight variation with frequency, the characteristic impedance for the growing wave is quite near to 20 Ω on gate drain and source, which allowing for the antiphase voltages makes the impedance between gate and drain nearly 50 Ω.

This value is dominated by the intrinsic FET and is little affected by geometry of microstrip lines, etc. It is of interest to note that balance feeding the TWF results in a reciprocal device. To make the transistor nonreciprocal and simplify the feed techniques, conventional feeding to gate only could be adopted with output on the drain. When operated in this configuration the growing mode is not as efficiently excited and the overall performance is severely degraded.

If perfect characteristic matching could be obtained, then only the growing mode would propagate. In practice, and particularly at high frequency, however, terminations will be nonideal. The model will cater for different reactive line terminations allowing different terminating circuits to be investigated, as well as including microstrip line end effects to the TWF electrodes. A linear combination of all the modes will propagate and be reflected at the boundaries. To account for this the full boundary value problem is solved for the general terminating conditions and this more general calculation is used in the results which follow.

TABLE I
Equivalent Circuit Parameters
(See Fig. 3.)

Parameter	Description	1 micron (GAT4)	0.6 micron (GAT6)	Typical for 1 micron FET
Ri/ohm o	Intrinsic source resistance	0.18×10^{-2}	0.9×10^{-3}	0.25×10^{-2}
gm/Sm^{-1}	Magnitude of intrinsic transconductance	180	140	99
t/S	Transit time	4×10^{-12}	4×10^{-12}	4×10^{-12}
Cds/Fm^{-1}	Intrinsic source-drain	0.5×10^{-9}	0.5×10^{-9}	0.5×10^{-9}
Rds/Fm^{-1}	ditto	0.27×10^{-2}	0.9×10^{-3}	0.25×10^{-2}
Rs/ohm o	Drain resistance (see Figure 3)	0.27	0.12	0.19
Cdg/Fm^{-1}	Intrinsic gate-drain	0.1×10^{-9}	0.33×10^{-10}	0.64×10^{-10}
Cgs/Fm^{-1}	Source-gate 'depletion'	0.15×10^{-9}	0.9×10^{-9}	0.19×10^{-9}
Rf/ohm o	Channel resistance	0.12×10^{-2}	0.294×10^{-2}	0.207×10^{-1}
ADDITIONAL PARASITICS				
Rbb/ohm o	Source-source electrode and drain to drain electrode	0.73×10^{-4}	0.23×10^{-4}	0.46×10^{-4}
Rd/ohm m^{-1}	Electrode resistance	100	100	1000
Rs/ohm m^{-1}		4000	4000	7000
Rb/ohm o		500	500	1000
C1/Fm^{-1}	Gate-drain capacitance due to T cross-section gate	0.0	0.0	0.0
C2/Fm^{-1}	Gate-source capacitance due to T cross-section gate	0.35×10^{-9}	0.35×10^{-9}	0.35×10^{-9}
C3/Fm^{-1}	Balancing overlay capacitance source to drain	0.14×10^{-9}	0.8×10^{-9}	2.2×10^{-9}
Rbb/ohm o	Source-earth bond wire resistance	0.2×10^{-3}	0.2×10^{-3}	0.2×10^{-3}
Lbb/Hm	Source-earth bond wire inductance	0.11×10^{-12}	0.11×10^{-12}	0.11×10^{-12}

V. Performance Predictions

The net gain of the device when balance fed to gate and drain and output into a balanced circuit is calculated by taking account of the total power into and out of *both* ports (gate and drain) when terminated. "Single end" feeding is also considered for comparison. Gain response curves are plotted in Fig. 5 for various configurations. The parameter values for the equivalent circuits for 1-μm (GAT4) and 0.6-μm (GAT6) devices used are given in Table I.

The results show that useful gain can be achieved over a wide bandwidth. Overall gain increases with total gatewidth and wider bandwidth is achievable with shorter gate lengths. The advantage gained by preferentially exciting the growing wave mode alone can be seen by comparing the balanced and "conventional" feed results. The *S*-parameters are also calculated by terminating a short device conventionally with 50-Ω lines.

VI. Device Fabrication

Traveling-wave FET devices of 1.2- and 3.0-mm (Fig. 1) active gate width have been fabricated on gallium arsenide epilayers. The n-type active layer was capped with an n^+ contact layer to reduce the parasitic source resistance R_S [13]. The initial fabrication stages of mesa and source–drain patterning were accomplished using standard photolithographic techniques. A low-resistance gate was achieved by fabricating a T cross section gate metallization using dielectric layers to support the overhanging extensions of the gate. This technique enabled a reduction in the measured resistance of the gate line to 7 Ω/mm.

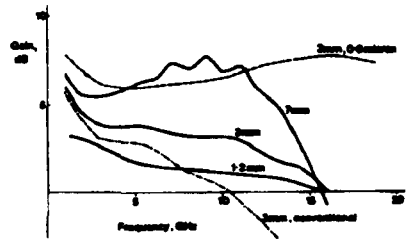


Fig. 5. Theoretical gain responses for various gate widths of 1 μm (GAT4) device with balanced feed (solid lines), a 3-mm-wide 0.6-μm (GAT6) device with balanced feed (dashed line) and a 3-mm-wide 1-μm (GAT4) device with conventional feeding (in on-gate only and out on-drain only) (dash-dot line).

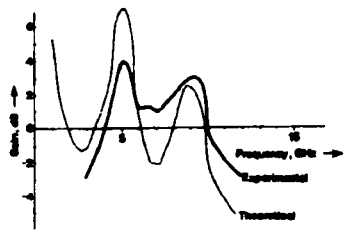


Fig. 6. Comparison of theoretical and experimental gain curves for a fabricated 3-mm-wide device with balanced feeds of 50-Ω impedance. The sharp "Fabry–Perot" peaks are a strong demonstration of traveling-wave action with mismatched boundaries. Results using 20-Ω impedance (not shown) show the expected flat band response indicated in Fig. 5 although the bandwidth at present is limited by the balun circuits.

It was shown using the computer model that reduction of this parasitic was desirable for achieving a growing wave.

The compensating overlay capacitors were fabricated using a dielectric and the earth connection was realized by a dielectric bridge over the gate line, making connection to the source electrode. The overlays were inserted at intervals which were small compared with the operating wavelengths.

Typical I_{dss} values of 200 mA/mm were measured with transconductances of between 95 mS/mm and 110 mS/mm, these values scaling with device length (total width for conventional FET's).

VII. RF Performance

The small-signal S-parameters of the TWF were measured by connecting the transistor as a conventional FET in a 50-Ω microstrip test circuit. The measurements were made on short TWF devices and at low frequencies to minimize distributed effects. From these measurements and dc measurements of transconductance, source resistance, and electrode resistance an equivalent circuit model was derived, which could be used in the computer program (see Table I).

TWF transistors of lengths 3.3 mm have been operated at X-band frequencies using both 50- and 20-Ω balun circuits. These balanced circuits were realized by using Lange couplers and meander lines to provide a −3-dB coupler with 180° phase imbalance. The measured frequency responses were compared directly with computed results for the device, taking into account the method of feeding the TWF. Fig. 6 shows the experimental and theoretical comparison for the device fed by 50-Ω baluns. The "Fabry–Perot type" of resonances can be clearly seen, and are a direct indication of traveling-wave action illustrating the reciprocal nature of the device, the growing wave being reflected and continuing to grow on its return. By reducing this impedance to 20 Ω, thereby improving the circuit-device match, both the experimental and theoretical plots show a reduction in the mismatch resonances.

VIII. Conclusions

The paper describes the design, theoretical modeling, and fabrication of a traveling-wave FET. The device shows the potential for wide-bandwidth (1–30 GHz) performance and high gain and would be most useful in medium-power applications. The fabricated devices have shown good agreement with the theoretical predictions and demonstrated the growing wave concept.

Appendix

With reference to Fig. 3, three coupled transmission line equations can be derived in terms of general impedance and admittance matrices. It is convenient to begin by ignoring the active circuits and additional parasitics and derive the equations for the simple passive three-line system. The admittances A_{ij} represent the capacitive coupling between lines i and j (or line to earth when $i = j$) and the impedances Z_{ij} contain the self and mutual inductances of the lines and the line resistances. All components are distributed and measured, per unit length.

Generalizing standard transmission line procedure, we apply Kirchoff's voltage and current laws to the element Δx at x and arrive at the familiar transmission line equation but in matrix form to take account of the multiple coupled lines

$$\frac{-d}{dx} V = ZI \tag{A1}$$

$$\frac{-d}{dx} I = YV \tag{A2}$$

where Z has components Z_{ij} and the voltage (V) and current (I) vector components represent each line. The new admittance matrix Y is defined in terms of the As by

$$Y_{ii} = \sum_{j} A_{ij} \tag{A3}$$

$$Y_{ij} = -A_{ij} \ (i \neq j). \tag{A4}$$

It is this definition which gives the relationship between the capacitance and charge matrices in Section III-A of the main text.

In order to generalize (A1) and (A2) to include the active circuit in Fig. 3 it is necessary to apply Kirchoff's current law to the nodes within the active circuit and rearrange the result into the same form as (A2). (Equation (A1) is unaffected by the active admittances.) The resultant active admittance matrix Y_a is then added to the passive matrix Y in (A2) to generalize (A2) for the active transmission line case. This last step is a general matrix form of the rule of addition of admittances in parallel.

We now choose a specific form for the wave solutions of the transmission equations. We choose

$$V_l = V_{lo} e^{j(k_l x - \omega t)} \tag{A5a}$$

The frequency dependence $e^{-j\omega t}$ is already taken care of in the definition of admittance and impedance. Thus

$$V_l = V_{lo} e^{jk_l x} \tag{A5b}$$

and also

$$I_l = I_{lo} e^{jk_l x}$$

where V_l (I_l) is the eigenvector, V_{lo} (I_{lo}) its magnitude, and k_l its complex eigenvalue (propagation constant or wave vector). (Note that this definition may differ from some reported in the literature.) Substituting (A5b) into (A1) and (A2) in turn and eliminating I_{lo} yields

$$k_l^2 V_{lo} = [-ZY]\ V_{lo}. \tag{A6}$$

Equation (A6) is the matrix eigenvalue equation whose solutions are the propagation modes of the three coupled active transmission lines.

ACKNOWLEDGMENT

The authors acknowledge valuable discussions with D. Herbert on the theory of modes of transmission lines, including active elements, and with G. J. Rees.

REFERENCES

[1] E. L. Ginzton, W. R. Hewlett J. I. Jasberg, and J. D. Noe, "Distributed amplification," *Proc. IRE*, vol. 36, pp. 956–969, 1948.
[2] W. Jutzi, "A MESFET distributed amplifier with 2 GHz bandwidth," *Proc. IEEE*, vol. 57, pp. 1195–1196, 1969.
[3] Y. Ayasli, R. L. Mozzi, J. L. Vorhaus, L. D. Reynolds, and R. A. Pucel, "A monolithic GaAs 1–13 GHz traveling-wave amplifier," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-30, pp. 976–981, 1982.
[4] E. W. Strid and K. R. Gleason, "A DC-12 GHz monolithic GaAs FET distributed amplifier," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-30, pp. 969–975, 1982.
[5] Y. Ayasli, L. D. Reynolds, J. L. Vorhaus, and L. Hanes, "Monolithic 2-20 GHz traveling wave amplifier," *Electron. Lett.*, vol. 18, pp. 596–598, 1982.
[6] Y.-A. Ren, G. Ruan, and H. L. Hartnagel, "Microwave structuring of MESFET electrodes for increased power and efficiency," in *IEDM Tech. Dig.*, pp. 684–687, 1981.
[7] A. J. Holden and C. H. Oxley, "Computer modeling of traveling wave transistors," in *Proc. Int. Conf. Simulation of Semiconductor Devices and Processes*, (Swansea, U.K., July 8–12, 1984).
[8] A. J. Holden, D. R. Daniel, and C. H. Oxley, "Distributed effects at high frequency in active and passive microwave circuits," in *IEE Colloquium Microwave Circuit CAD Techniques*, U.K. Dig. no. 1983/38, pp. 5/1–5/5, Apr. 1983.
[9] A. S. Podgorski and L. Y. Wei, "Theory of traveling wave transistors," *IEEE Trans. Electron Devices*, vol. ED-29, pp. 1845–1853, 1982.
[10] C. J. Wei, "Novel design of traveling-wave FET," *Electron. Lett.*, vol. 19, pp. 461–463, 1983.
[11] P. Silvester, "TEM wave properties of microstrip transmission lines," *Proc. IEE*, vol. 115, pp. 43–48, 1968.
[12] C. A. Liechti, "Microwave field effect transistors," in *IEEE Trans. Microwave Theory Tech.*, vol. MTT-24, pp. 279–300, 1976.
[13] Hower and Bechtal, "The GaAs field effect transistor," *Applications and Devices*, vol. 7, 1971.

Travelling Wave Gallium Arsenide Transistors

by A J Holden and C H Oxley

Introduction. Transmission line structures, as has been demonstrated by the use of travelling wave tubes in radar systems, can have very low losses, close control of phasing and uniform properties over a wide range of frequencies [1]. The high frequency performance of a field effect transistor (FET) is limited by the magnitude of its input capacitance. A transmission line can be used to combine a number of FETs in parallel, so as to increase the gain, but to feed them sequentially so that the limitation in bandwidth due to their high capacitance is avoided.

Since only small dimensions are available in semiconducting devices, transmission line structures within them can only be a few millimetres in length so that their realisation has had to await some necessary advances in technology.

The design of suitable structures by rule of thumb would be prolonged and expensive because of their complexity and the difficulty of developing an intuitive approach to their behaviour. Mathematical modelling is therefore essential to the design of experimentally realisable devices.

The two structures that have led up to the present development are the travelling wave FET (TWF) [2] and the travelling wave amplifier (TWA) [3]. A TWF device developed at Caswell is shown in *Fig. 1*. It consists of a very wide FET (2–7mm) structure in which waves propagate across the width of the device using the source,

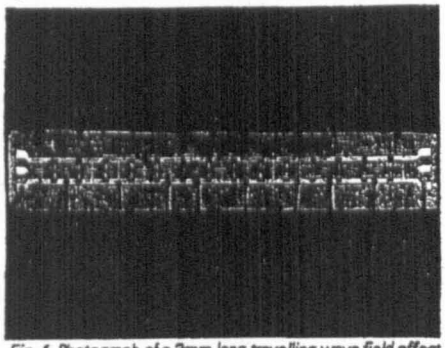


Fig. 1. Photograph of a 3mm long travelling wave field effect transistor fabricated at Caswell.

gate and drain electrodes (or extensions of them) as microstrip transmission lines. Due to the active nature of its substrate a large depletion capacitance is present under the gate line. In order to keep the waves on the gate and drain travelling together and driving the transistor continuously across its width, compensating capacitors are distributed along the drain, which can be connected to the earthed source line by overlays.

The TWA approach, as shown in *Fig. 2* uses separate FET units connected by transmission lines. In this case

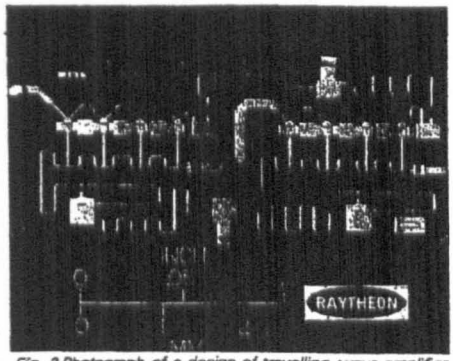


Fig. 2.Photograph of a design of travelling wave amplifier. (Courtesy of Raytheon Research Division)

the slow waves on the gate are balanced by making the drain transmission line longer than the gate transmission line between active elements.

Although these two approaches operate in different ways they promise similar performances in broad-band, medium power applications. Their advantages and limitations are discussed below. A fundamental development in theoretical modelling has made a unified approach to the TWF and TWA designs possible and has resulted in a new device, the linear gate transistor (LGT) which combines the advantages of its predecessors and avoids many of their limitations. The new model depends on an extension of the well established transmission line theory to an active transmission line, but the discussion will start with coupled passive lines.

Coupled Passive Lines. We first extend the familiar transmission line theory to a number of coupled lines with a common ground plane. Although the general solution would require a full field solution of Maxwell's equations we confine our attention to the lowest order 'quasi T.E.M.' modes. At this level a distributed equivalent circuit model can be used to generate the transmission line solutions and such a model is most convenient for generalising to the active line case. *Fig. 3* depicts a differential element of the distributed circuit model for three coupled lines with a common ground. Further

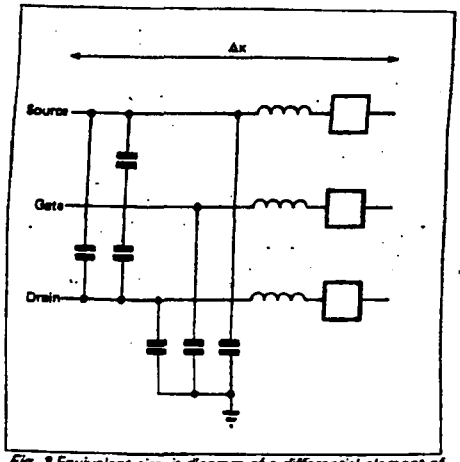


Fig. 3 Equivalent circuit diagram of a differential element of three coupled microstrip lines.

lines could be added in an obvious way. This circuit is analysed by analogy with the usual single line case. We apply Kirchhoff's voltage law along each line producing three simultaneous equations which can be expressed as a matrix equation:

$$-dV(x)/dx = ZI(x) \quad (1)$$

Here Z is the matrix of line impedance, self and mutual.

The components of vector V are the 3 line voltages and the components of vector I are the 3 line currents. Equation (1) will be recognised as a vector form of one of the traditional transmission line equations.

The second familiar equation relating differential current to voltage is obtained by applying Kirchhoff's current law at each node producing three simultaneous equations which we express as:

$$-dI(x)/dx = YV(x) \quad (2)$$

where Y is a matrix of the capacitive admittances.

We now manipulate (1) and (2) to obtain the eigenmode equations. The time dependence has already been defined as oscillatory with frequency ω in our definition of impedance and admittance. We now define the spacial dependence in the form of plane waves with wavevector k in an analogous way to a single transmission line.

$$V = V_0 e^{jkx} \quad (3a)$$

$$I = I_0 e^{jkx} \quad (3b)$$

In general k will be complex, its real part giving the traditional propagation constant or wavenumber for the wave. Its imaginary part will describe the loss in the line (note that a positive imaginary part leads to an exponentially decaying factor).

Using (3) in (1) and (2) and rearranging we finally obtain

$$(-ZY)V(x) = k^2V(x) \quad (4)$$

which is a complex eigenmode equation analogous to the single line expression for wavevector $k = \omega\sqrt{LC}$. For our three line example three solutions for k^2 and V will exist giving six values of k. These solutions represent three modes travelling in the positive x direction and three in the negative x direction. They are the solutions to the infinite line problem. If the line is terminated at the ends, giving boundary conditions, the total solution will be formed from a linear combination of these modes. That there should be three modes in each direction can be understood if we separate the three lines well apart. Then each independent transmission line will carry a single mode in each direction. As the lines are brought together the fields couple and a new set of three normal modes appear in the conventional way.

Coupled Active Lines. In order to model distributed transistors the active components associated with the gate channel region have to be incorporated. In lumped element models an equivalent circuit is used which features a current source modulated by the source-gate voltage. Because we have set up our coupled line theory in terms of equivalent circuits it is now possible to incorporate a distributed form of the intrinsic circuit model of a FET. *Fig. 4* shows the differential element of such a circuit where now all the components are taken 'per unit length' of device. This length of transmission line in the TWF geometry corresponds to conventional

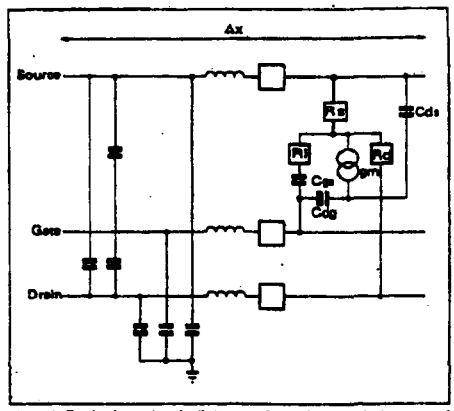


Fig. 4 Equivalent circuit diagram of a differential element of an active transmission line system.

gate 'width'. In the TWA however a complication arises because the various transmission lines differ in length between lumped active elements. The differing lengths can be taken into account by scaling and projecting positions on the gate line to scaled positions on the drain line. The active regions, though lumped at points on the line, are assumed to be distributed evenly along the respective lines, an approximation which is valid provided that the distances are all small compared with the wavelengths in question. This approximation is the essence of travelling wave device theory and is valid for most frequencies of interest, the approximation is applied to all lumped elements in the devices including the periodically arranged overlay capacitors in the TWF geometry.

With the above provisos the circuit in *Fig. 4* can be analysed in the same way as that in *Fig. 3*. The voltage law is the same, yielding equation (1) identically. The current law is complicated by the large number of additional nodes that occur in the intrinsic circuit. However, the analysis, though messy, is tractable and we arrive at an equation similar to (2) but with an admittance matrix which is a sum of the passive matrix in (2) and a new active matrix dependent on the intrinsic cicuit. The appearance of such a form is not surprising as it is simply a matrix generalisation of the addition of admittances in parallel. With this modified form for **Y** the analysis carries through and we arrive again at equation (4). The scaling referred to above for the TWA case modifies the matrices but leaves the form of the equations unchanged with x now measured along the drain line and the problem expressed as a 3 x 3 or 2 x 2 matrix depending on whether a continuous source line is incorporated or not. This scaling, though based on a much simpler published analysis for TWA [3] is the key generalisation developed at Caswell which enables us to model all TWA devices in detail and evolve a totally new design concept for the Linear Gate Transistor described later on.

Equation (4) now gives the eigenmodes for the coupled active transmission lines and its solution together with appropriate boundary conditions forms the core of the design software developed at Caswell.

The Travelling Wave FET. After much theoretical discussion, a prototype TWF was designed by H.D. Rees of R.S.R.E., Malvern, and engineered into a working device at Caswell. This involved an extension of Rees' theory, to form a suite of design programs, and a solution to the formidable problem of fabricating a wide, but low resistance, gate. The TWF may be regarded as a stretched FET with expanded geometry, to allow for source and drain transmission lines, and a T cross-section gate (*Fig. 1*).

Theoretical. *Fig. 5* shows the basic layout of a section of a TWF. All electrodes are parallel with periodic feeds connecting source and drain to the active regions near to the gate. As described in the introduction the large depletion capacitance of the active device has to be compensated and this is done in the TWF by periodically arranged capacitor pads on the drain connected to the source via an overlay conductor as shown. The spacing of the capacitors is small compared with the propagation wavelength. Using the analysis described above the modes of the device can be evaluated and these are shown in *Fig. 6*. Only the voltage phasor diagrams are shown but the current vectors are very similar in direction implying that the mode impedances are virtually real, an important advantage in matching the device. The vectors are not particularly sensitive to frequency in the band of interest (1-20GHZ).

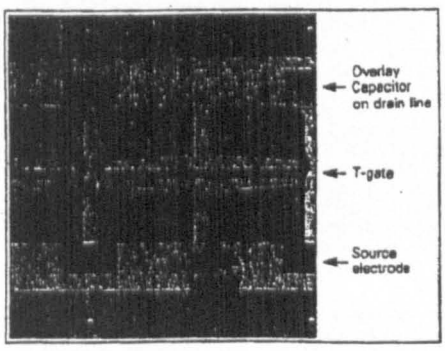


Fig. 5. Detail of the travelling wave FET construction.

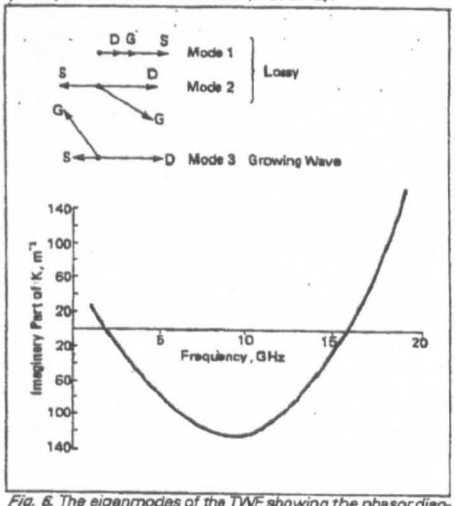


Fig. 6. The eigenmodes of the TWF showing the phasor diagrams and the imaginary propagation constant for the 'growing wave'.

Inspection of the propagation parameter k shows that the first two modes are lossy (having a positive imaginary part at all frequencies) but that the third mode has a negative imaginary part of k over some of the band (*Fig. 6*) such that according to equation (3), it grows as the wave travels across the device. That such a growing wave can exist is due to the active nature of the device, and the fact that the amplified power which appears traditionally on the drain electrode is fed back into the lossy gate electrode via the mutual inductance. This inductance is deliberately enhanced in the TWF by separating the main source and drain transmission electrodes from the intrinsic FET structure around the gate to leave gaps in the metallisation where the magnetic field can penetrate. We note that the gate and drain voltages in this mode are virtually in antiphase so that the mode drives the device continuously as it passes down the transmission line and so draws power. In both of the other modes the gate and drain are in phase so that the device is not driven and power is simply dissipated in the device and transmission line parasitics.

If we make a very wide (in conventional FET parlance) TWF and excite the growing wave, the voltage on gate and drain will continue to grow so that gain will increase

monotonically with device width (based on small signal theory) and is, ultimately, only limited by non-linear effects or, more commonly, oscillations due to reflections at mismatched boundaries. In order to achieve this the gate and drain have to be well matched and fed in antiphase. It turns out that the impedance of the growing wave is around 20 ohm (to ground on each line) and it is difficult, technologically, to achieve these feed conditions over a wide bandwidth. In practice some of the lossy modes will be unintentionally launched wasting some of the power and, more seriously, impedance mismatch will occur, reflecting the growing wave. By its nature the TWF is reciprocal and a growing wave reflected at the far end will continue to grow on its return producing very strong 'Fabry-Perot' type oscillations and possible instability. Such oscillations are a prominent feature of TWF operation and are the ultimate limit on performance. Even if perfect matching can be achieved it is necessary to fabricate gates of 0.7μm in length with widths in excess of 10mm in order to obtain useful gain (in excess of 10dB) over a wide bandwidth (say 1-20 GHz). Typical theoretical predictions for different TWF configurations are shown in *Fig. 7*.

Experimental. The travelling wave FET (*Fig. 1*) has been fabricated using the normal processing techniques for conventional GaAs FETs and integrated circuits. The ohmic source and drain contacts consist of successive layers of indium, germanium and gold with the outer gold layer a few micrometres thick in order to

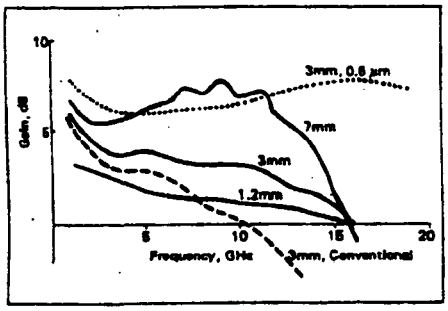


Fig. 7. Theoretical performance predictions for the TWF showing variation in gate length (μm) and gate width (mm).

minimise the resistance of the electrodes. A standard etch channel technology has been adopted to reduce the source resistance. As in conventional FETs this parasitic resistance has an influence on both the gain and noise performance of the device. Unlike conventional transistors, the TWF consists of one gate stripe, up to 10mm wide, and 1μm long. To overcome the resulting high gate resistance a 'T' – Gate technology has been developed. The upper cross of the 'T' is some 10μm wide and this reduces the gate resistance to less than 10 ohms/mm (*Fig. 5*). A polyimide layer provides dielectric support to the widened sections of the 'T'-shaped Gate.

To achieve travelling-wave FET action it is necessary for the source – drain capacitance to be comparable to the source-gate depletion and parasitic capacitance. Capacitors are, therefore, placed at regular intervals along the TWF between the source and drain transmission lines. *Fig. 5* shows a close-up photograph of a section of the TWF in which the overlay capacitor can be clearly seen. The capacitors take the form of pads of silicon nitride on the drain metallisation with a metal connector from the source electrode crossing the gate region and forming the top plate of the capacitor.

Travelling Wave Amplifiers compared with Travelling Wave FETs. 'Travelling Wave' or distributed amplifiers of different types have been of interest for a long time but concentration has focussed more recently on monolithic designs using integrated FET and microstrip structures (3). Superficially the TWA looks very similar to the TWF consisting of active units connected by separate gate and drain transmission lines. *Fig. 2* shows a photograph of such a device. On closer inspection it can be seen that:

(i) The individual active gates are mounted transversely to the main transmission lines[1]. This is not particularly significant as the active properties are assumed to appear as if distributed along the lines but the conventional narrow gate metallisation has a high resistance and is an important parastic in the TWA (the TWF has a low resistance T cross-section structure along all active regions).

(ii) The gate and drain transmission lines are separately meandered and have different lengths between active units.

(iii) As a result of (ii) the inductive coupling between the gate and drain transmission lines is negligible.

(iv) Power is fed into the gate at one end and taken from the drain at the other as in a conventional FET; the opposite ends of these lines are terminated in characteristic impedances.

The reason for the meandered gate and drain lines is to balance the waves on these two lines. In the TWA the slower waves on the gate caused by the high depletion capacitance are matched on the drain by making the drain line longer than the gate line. Qualitatively there should be no difference between this balancing method and the overlay capacitor method used in the TWF. There is an important quantitative advantage in the TWA technique as it has a higher transmission line impedance than the TWF, leading in practice to higher gains for devices with gate lengths greater than 0.8μm and medium transmission line lengths (less than 4mm)[14].

The superficial similarities between TWA and TWF cover a much more fundamental difference in their operation. In the TWF inductive coupling between the gate and drain lines causes a feed-back of power from the drain into the gate, compensating for the inherently lossy gate line and producing the growing mode. No such coupling occurs in the TWA and indeed for the mode of operation of existing TWAs any inductive coupling would *degrade* performance. There is no growing wave in a TWA device. Gain in the TWA occurs in a similar way to gain in a conventional FET, although the operation of a conventional FET is not normally thought of in these terms. By applying the theory described above to the TWA configuration we find that the eigenmodes are

similar in form to those of the TWF (modes 1,2, and 3 in *Fig. 6*) but all are lossy and the gate voltages are smaller. Mode 3, however, has much lower loss than modes 1 and 2. By feeding the TWA into the gate a linear combination of modes 2 and 3 in *Fig. 6* is generated by adding them together in roughly equal amounts but with opposite sign. This yields a finite gate voltage but the two large drain voltages cancel to satisfy the drain boundary condition. These two modes travel down the device until the high loss mode is damped away, at which point the maximum gain may be extracted since only the drain voltage for the low loss mode is left and gives a large output voltage.

Adding further FET units is counterproductive as the remaining mode can only decay further as it travels along the transmission line. A separate analysis of a conventional FET geometry treated as a short transmission line reveals a similar process with high and low loss modes 'propagating' along the width of the device. Of course for very narrow FETs the concept of mode propagation is not so useful but the basic mechanism should be observable in wider structures.

The gain mechanism in the TWA is thus very different to that of the TWF and, although its increased impedance gives it a distinct advantage for transmission line lengths of less than 4mm, the total useable length in the TWA is limited by the decay length of the lossy mode whereas the growing wave in the TWF will continue to show improvements. The main disadvantage of the TWF is that more than 10mm of device is needed to show worthwhile gain. Its reciprocal nature results in 'Fabrey-Perot' oscillations due to mismatching boundaries and its usefulness is further limited by the need for the wide bandwidth low loss balun circuits required to launch the growing mode.

The Linear Gate Transistor. The linear gate transistor (LGT) is a design of device (*Fig. 8*) which combines the distinct advantages of the higher drain impedance and single end feeding of a TWA with the all important drain

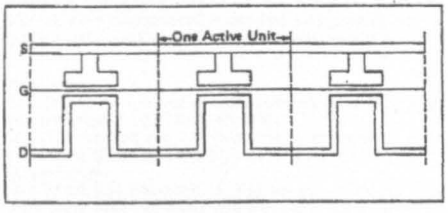


Fig. 8. Schematic drawing of a linear gate transistor.

to gate inductive feed-back which leads to growing wave action. Instead of using separate FET devices with local gates transverse to the main transmission lines the Linear Gate Transistor earns its name by using a single continuous gate stripe which runs parallel to the drain line in the active regions in sufficient proximity to provide inductive coupling. This coupling is less than in the TWF because the drain is meandered between active elements to provide phase balance (no overlay capacitors are used!) but a growing wave can be produced provided that the gate length is shorter than about 0.7μm. This device is single end fed (to the gate only) and hence launches a high loss wave and a growing wave. After about five active sections the low loss wave has vanished leaving a large voltage on the drain (this is the conventional TWA gain mechanism enhanced by the growing wave action) however, unlike the TWA, the LGT can now have further active sections added and the growing wave continues to grow displaying the monotonic increase in gain with overall gate width (the TWA degrades for gate widths wider than the optimum for conventional gain). Thus a wide-band (1-30 GHz) high gain (> 10dB) device can be made without the complication of cascading a series of narrow TWAs [3].

The all-important gate line resistance is reduced by a T cross-section line similar to that in the TWF and in addition the whole line is widened between active regions where FET action is not operative (see *Fig. 9*).

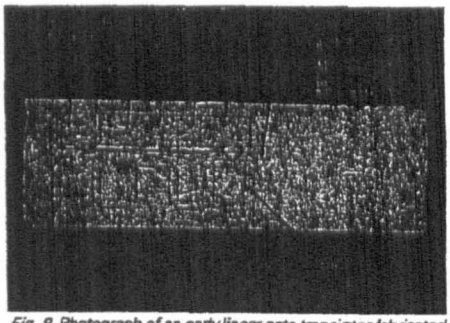


Fig. 9. Photograph of an early linear gate transistor fabricated at Caswell.

The resulting structure is much simpler than the TWA with potential for improved r.f. performance because of the growing wave action. It shows higher gain per unit gatewidth than the TWF because, in particular it uses conventional TWA gain at low frequency and growing waves at higher frequency and does not require the complex balun circuits. *Fig. 10* shows the predicted performance of LGT devices for different geometrical configurations. Such predictions are made possible because of the unified nature of the theoretical modelling which scales the inductive coupling as well as the intrinsic active elements to allow for the meandered drain line.

The fabrication of this device is simpler than for the TWF and TWA, in that the transistor is a planar structure not requiring 'via' technology or the balancing capacitors. The complication introduced by the 'T' gate technology, is a small price to pay for the inherent wideband performance.

The Future. The LGT device represents a major advance in travelling wave devices providing wide-band high gain and medium power operation. It has potential applications in wideband receivers and wideband medium power drivers for power tube amplifiers. The wide, flat bandwidth and compact design should enable

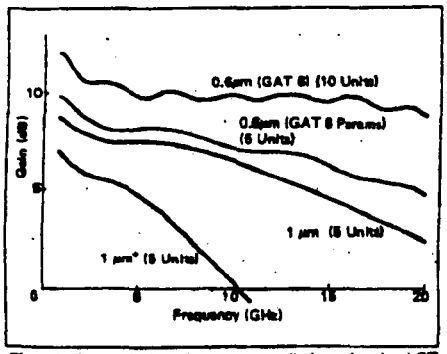


Fig. 10. Theoretical performance predictions for the LGT showing how the growing wave improves performance at shorter gate lengths.

it to slot conveniently into diverse situations in the growing III–V technology. Our advanced modelling software allows many designs to be tested and optimised and, with the major new developments in the technology, will allow the manufacture of new devices with improved r.f. performance.

There has also been valuable spin-off from both the theoretical and technological programmes involved in this development. The software is being used to investigate distributed effects in such diverse areas as power and high frequency FETs, multiple coupled line structures in integrated circuits and, more recently, in the sub-emitter region of a bipolar transistor. The low resistance gate technology is expected to find applications in power and other FET designs.

Acknowledgements. Part of this work was carried out with the support of the Procurment Executive, Ministry of Defence, sponsored by DCVD.

The authors would like to thank H.D. Rees and G.J. Rees for many helpful discussions, I. Davies and D.R. Daniel, who fabricated the devices and J. Joshi for his advice and practical assistance in measurements.

References.

1. G.W. McIver. A travelling-wave transistor. Proc. IEEE (Correspondence). *53*. p.1747-1748, 1965.
2. A.S. Podgorski and L.Y. Wei. Theory of travelling wave transistors. IEEE Trans. ED.*29*. p.1845-1853, 1982, and references therein.
3. Y. Ayasli, L.D. Reynolds, J.L. Vorhaus and L.K. Hanes. 2-20 GHz GaAs travelling wave amplifier. IEEE Trans. MTT *32*. p.71-77, 1984. E.W. Strid and K.R. Gleason. A DC-12 monolithic GaAs FET distributed amplifier. IEEE Trans. MTT *30*. p.969, 1982.
4. A.J. Holden and C.H. Oxley. Computer modelling of travelling wave transistors. Proceedings of the International Conference on simulation of semiconductor devices and processes, University College, Swansea. p.319-329, 1984.

APPENDIX 6(continued)

Reference to these published works in the text is denoted by the letter C, for example [C1]:-

9) C.H.Oxley and M.J.Uren 'Measurement of unity gain cut-off frequency and saturation velocity of a GaN HEMT transistor', IEEE trans ED February 2005. (Hard copy not included).

10) C.H.Oxley 'A novel method for measuring the source resistance R_s of a GaN HEMT device over bias conditions (V_{gs}, V_{ds}). Electronics Letters, 4th March 2004, vol.40, no.5, pp344-346.

11) C.H.Oxley 'Gallium Nitride: the promise of high RF power and low microwave noise performance in S and I band'. SSE 48, (2004), pp 1197-1203.

12) C.H.Oxley 'Noise Performance and Applications of Gallium Nitride (GaN) HEMT Transistors' Proc. Wireless Design Conference, London UK, pp 19-22, May 2002. (Hard copy not included).

13) C.H.Oxley 'A simple approach including gate leakage for calculating the minimum noise performance of GaN HEMTs' Microwave and Optical Technology Letters, Volume 33, nos. 2, pp113-115, April 2002.

14) *C.H.Oxley 'Calculation of minimum noise figure using the simple Fukui equation for gallium nitride (GaN) HEMTs' Solid State Electron, 45,pp 677-682, 2001.

15) *C.H.Oxley and O.Buiu 'Comparison of wide band gap and III-V semiconductor devices' Microwave Engineering Europe, vol 7, nos.10 pp, Nov 2001. (Hard copy not included).

16) C.H.Oxley, S.Redfern, B.Prime, T.Brown, D.Spencer, D.Dawson, J.Bird, and G.Hilder 'An Automotive 77GH_z Radar Sensor Designed for Volume Manufacture' Conference Proceedings of Telematics Automotive 2000, Volume 1, pages 10 t0 17, April 2000. (Hard copy not included).

reverse bias. This indicates that the δ-doped p^+ layer is fully depleted under thermal equilibrium [4, 5] and that the current flow is predominantly controlled by thermionic emission over the barrier in both forward and reverse directions.

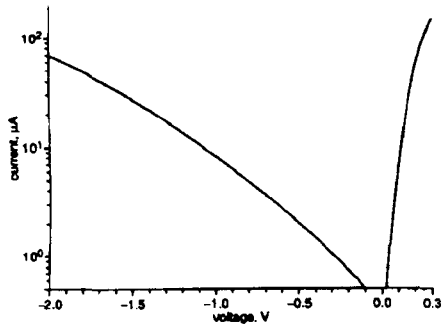


Fig. 2 *I–V characteristics of zero-bias PDB detector diode (3 × 9 μm) at room temperature*

Based on the I–V measurements [6], the barrier height and ideality factor of the device are found to be 0.34 eV and 1.19, respectively. This barrier height is about 0.04 eV higher than that designed. The difference is consistent with small deviations from growth specifications: either the thickness of the shorter intrinsic layer (20 nm), or sheet density of the δ-doped p^+ layer.

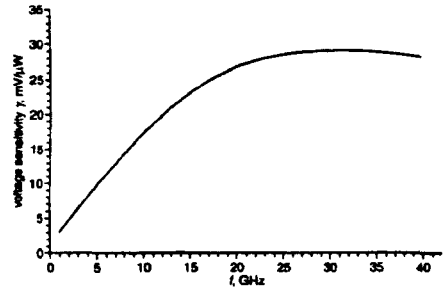


Fig. 3 *Voltage sensitivity of PDB detector diode*

Since a detector diode can be considered as a current source across the diode video impedance, the voltage sensitivity is the product of the current sensitivity and the derivative of current with respect to voltage [2, 7]. The voltage sensitivity for our zero-bias PDB detector diode against frequency is illustrated in Fig. 3. The diode RF parameters were extracted from on-wafer *S*-parameters measurement, which was carried out from 40 MHz to 40 GHz using an HP85107A network analyser. The effects of a load resistor of 100 kΩ and reflection loss were taken into account assuming the detector diode to be working under a 50 Ω system. It can be seen that these PDB diodes are capable of giving excellent power detection performance and reach their maximum at a frequency of approximately 32 GHz, with voltage sensitivity of 29 mV/μW.

Table 1 shows the voltage sensitivity of Agilent's HSCH-3486, EEV's PDBGB322 and our PDB detector diodes. It can be seen that at 16 GHz the voltage sensitivity of this work is about eight and near three times higher than that of HSCH-3486 and PDBGB322, respectively. At 35 GHz, our device outperforms PDBGB322 with ten times higher voltage sensitivity.

Table 1: Comparison of voltage sensitivity of PDB detector diodes

Diodes	γ (mV/μW) at 10 GHz	γ (mV/μW) at 35 GHz
KCL (3 × 9 μm²) PDB diode	17.4	28.6
HSCH-3486 (Agilent Technologies) [7]	2.1	
PDBGB322 (e2v Technologies) [2]	6.5 (at 9.375 GHz)	2.6

Conclusions: Microwave/millimetre-wave zero-bias GaAs PDB detector diodes have been designed, fabricated and evaluated. The device with active region of 3 × 9 μm has voltage sensitivity as high as 29 mV/μW at 35 GHz, and significantly outperforms currently available devices (Agilent's and EEV's). Since the device has higher voltage sensitivity, it can detect lower RF power providing the device with significantly higher dynamic range for microwave/ millimetre-wave applications.

Acknowledgment: This work was supported by the UK Engineering and Physical Sciences Research Council (Grant No. GR/R12336/01) and Nuffield Foundations.

© IEE 2004 *8 January 2004*
Electronics Letters online no: 20040217
doi: 10.1049/el:20040217

V.T. Vo, C.N. Dharmasiri, S.C. Subramaniam and A.A. Rezazadeh (*Department of Electrical Engineering & Electronics, UMIST, PO Box 88, Manchester M60 1QD, United Kingdom*)

E-mail: tuyen.vo@umist.ac.uk

Z.R. Hu and K.L. Koon (*Department of Electronic Engineering, King's College, University of London, Strand, London WC2R 2LS, United Kingdom*)

References

1 Malik, R.J., Aucoin, T.R., Ross, R.L., Board, K., Wood, C.E.C., and Eastman, L.F.: 'Planar doped barrier diodes in GaAs by molecular beam epitaxy', *Electron. Lett.*, 1980, 16, pp. 836–837
2 Kearney, M.J., and Dale, I.: 'GaAs planar doped barrier diodes for mixer and detector applications', *GEC J. Res.*, 1990, 8, pp. 1–12
3 Kearney, M.J., Condie, A., and Dale, I.: 'GaAs planar doped barrier diodes for millimetre-wave detector applications', *Electron. Lett.*, 1991, 27, pp. 721–722
4 Tuyen, V.V., Hu, Z.R., Rezazadeh, A.A., and Wu, Y.H.: 'Ion implanted camel diodes fabricated on high resistivity silicon for microwave and millimetre-wave applications', *Electron. Lett.*, 2002, 38, pp. 1228–1229
5 Hutchinson, S., Kelly, M.J., Gwilliam, R., Sealy, B.J., and Carr, M.: 'Bulk unipolar diodes formed in GaAs by ion implantation', *Nucl. Instrum. Methods Phys. Res.*, 1999, B148, p. 478
6 Tuyen, V.V., Nadia, F., Hu, Z.R., and Rezazadeh, A.A.: 'Experimental verification of barrier height temperature dependence in GaAs planar doped barrier diodes', *Electron. Lett.*, 2003, 39, pp. 324–326
7 'The zero bias Schottky detector diode', Application Note 969, Agilent Technologies

Method for measuring source resistance R_s in saturation region of GaN HEMT device over bias conditions (V_{gs}, V_{ds})

C.H. Oxley

To accurately model distortion effects using a large signal model the variation of all the elements of the equivalent circuit model under bias conditions are required. A technique is presented to extract the source resistance R_s under bias conditions for the aluminium gallium nitride/gallium nitride (AlGaN/GaN) HEMT. The source resistance R_s is found to decrease as V_{ds} is increased, implying that the conduction channel becomes wider, which indicates a parallel conduction path to the 2D electron-gas.

Introduction: Gallium nitride is a particularly interesting wide-bandgap semiconductor material offering potential for high-frequency high-power transistors, particularly in the application of broadband wireless base station applications in 3G, multi-video distribution systems (MVDS), and multi-wireless systems (MWS). The material has a high E_a breakdown field ($E_a = 330$ MV/m) and a simulated [1] high saturation velocity ($v_s = 2.5 \times 10^5$ m/s). The maximum unity gain cutoff frequency f_t is primarily dependent on the saturation velocity v_s of the HEMT device. A rule of thumb suggests that for power transistors, the maximum useful operating frequency $f_{max} < 0.5 f_t$ to operate a power device in the 25–33 GHz band, requires the f_t to be around 70 GHz.

With increasing network capacities, more complex modulation schemes are required which will necessitate very linear transmitters to minimise distortion. To investigate the linearity of the high-power HEMT, large signal models will be required in which all the elements can be described as a function of the gate source (V_{gs}) and drain source (V_{ds}) bias conditions. One parameter, that is particularly difficult to extract, is the source resistance (R_s). A number of publications have also suggested that the source resistance of a GaN HEMT significantly varies under large signal conditions [1, 2]. This Letter describes a routine for extracting this parameter under all bias conditions (V_{gs} and V_{ds}).

Device structure: An aluminium gallium nitride/gallium nitride (AlGaN/GaN) HEMT transistor was fabricated at the QinetiQ facility within the UK. The transistor consisted of a nominal 0.25 μm gate length with a metallised T-profile to minimise the parasitic gate resistance R_g. The total gate width was 100 μm, and consisted of two unit gate-widths of 50 μm in a 'pi' configuration. The structure was fabricated on an SiC substrate with AlN buffer region and passivated with silicon nitride (Si_3N_4).

The *s*-parameters of the transistor were measured by QinitiQ over a wide range of bias conditions from 0.25 to 50 GHz, using an Agilent network analyser and an RF probe station. The device had a measured pinch-off voltage (V_p) of approximately −6.5 V.

Device measurements: The f_t of the 0.25 μm gate length transistor was measured by transforming the *s*-parameters to *h*-parameters, and plotting h_{21} against frequency, extrapolating the h_{21} parameter (−20 dB/decade) and reading the frequency at the 0 dB point. A set of curves (Fig. 1) was produced for a wide range of bias conditions.

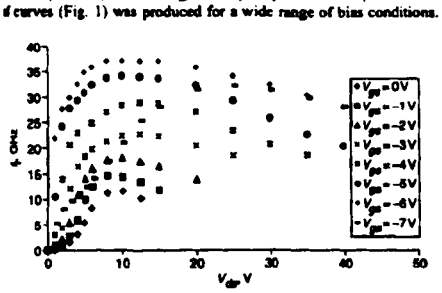


Fig. 1 *f_t against V_{ds} for different V_{gs}*

From the small signal *s*-parameters the transistor extrinsic and intrinsic parameters were de-embedded using similar techniques as described in [3]. The *s*-parameters were first transferred to *Y*-parameters and the parasitic pad capacitance, gate source (R_{gs}) and drain gate (R_{dg}) shunt resistances de-embedded. The parameters were then transformed to *Z*-parameters and an estimate of the drain (R_d), source (R_s), and gate (R_g), resistance were obtained by extrapolating the high frequency values to low frequencies and solving the simultaneous equations to obtain $R_d = 10\ \Omega$, $R_s = 8.5\ \Omega$ and $R_g = 0.46\ \Omega$. A best-fit to Z_{11} was then performed to 10 GHz to obtain a value of 0.03 pH for the gate inductance (L_g), which will be dependent on the depletion layer under the gate, and for a HEMT device can be considered as a constant [4].

These extrinsic circuit parameters were used to obtain a set of de-embedded *Y*-parameters, which would be related to the intrinsic parameters of the transistor. The parameters included the gate source capacitance (C_{gs}), gate drain capacitance (C_{gd}), drain source capacitance (C_{ds}) and drain source output conductance (g_{ds}) and were found to be almost invariant with frequency. The channel resistance (R_i), transit time (τ), and g_m were extracted from *s*-parameters, using the more accurate expressions [4]. In particular, the expression $g_m = [(Real(g_m))^2 + Imag(g_m))^2]^{0.5}$ was used to help to minimise effects which could be attributed to frequency dispersion.

Extraction of source resistance R_s: Provided $\omega_m^2 C_{gs}^2 [R_i + R_g] \ll 1$ and the gate and source inductive reactance at the measurement frequency is very small ($|\omega_m L_g|$ and $|\omega_m L_s| \ll R_g$, then the following expressions resulting from feedback can be used:

$$C_{gsext} = C_{gsint}[1 + R_{so} g_m] \quad (1)$$

$$g_{mext} = \frac{g_{mint}}{1 + R_{so} g_{mo}} \quad (2)$$

where C_{gsext} and g_{mext} are the 'extrinsic' values and C_{gsi} and g_{mi} are the intrinsic values, respectively. R_{so} is the already known de-embedded source resistance.

If the source resistance varies by $\pm \Delta R_s$ due to bias point then the following forms of equation will apply:

$$C_{gsi} = C_{gsext}[1 \pm \Delta R_s g_{mext}] \quad (3)$$

$$g_{mi} = \frac{g_{mext}}{1 \pm \Delta R_s g_{mext}} \quad (4)$$

where C_{gsi} and g_{mi} are the actual extrinsic values for the gate source capacitance and transconductance.

The f_t of the transistor can now be calculated by substituting (3) and (4) into (5)

$$f_t = \frac{g_{mi}}{2\pi(C_{gsi} + C_{gdi} + C_{pad})} \quad (5)$$

resulting in a quadratic equation in ΔR_s, and provided f_t is known, the quadratic equation can be solved for ΔR_s:

$$\Delta R_s^2 C_{gs} g_m + \Delta R_s [2C_{gs} + C_{gd} + C_{pad}] + \left\{ \frac{C_{gs} + C_{gd} + C_{pad}}{1 g_{mo}} \right\} - \frac{1}{\omega_t} = 0 \quad (6)$$

It is now possible to write R_s as a function of bias setting

$$R_s(V_{gs}, V_{ds}) = R_{so} \pm \Delta R_s \quad (7)$$

Discussion of results: Fig. 2 shows the variation of R_s in the saturation region with V_{ds} and V_{gs}. The classical decrease in source resistance is seen with increasing V_{ds} when $V_{gs} = -6$ V.

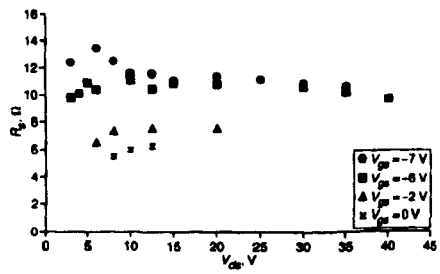


Fig. 2 *Variation of source resistance R_s with V_{ds} and V_{gs}*

At −7 V just into pinch-off the access resistance increases at low V_{ds}; this is not surprising since the 2D-sheet resistance will be high under the gate and spreading into the source and drain access regions. Perhaps the interesting observation is that at high V_{ds} the access resistance improves.

At high V_{gs} the access resistance appears to be lower, which would suggest that the carrier conduction is spread over a larger cross-section of the conducting channel. The increase in cross-section may be due to a parallel conduction path to the 2D electron-gas layer [5] and the carriers in both regions having velocities, which are of similar order of magnitude. The parallel conduction path may be in either the gallium nitride or the aluminium gallium nitride layer [5].

© IEE 2004 *9 January 2004*
Electronics Letters online no: 20040236
doi: 10.1049/el 20040236

C.H. Oxley (*De Montfort University, Leicester LE1 9BH, United Kingdom*)
E-mail choxley@dmu.ac.uk

References

1 Ren, F., and Zolper, J.C.: 'Wide energy bandgap electronic devices' (World Scientific, London, UK, 2003)
2 Trew, T.J.: 'AlGaN/GaN HFET amplifier performance and limitations', MTTS, CD-ROM, 2002, pp. 1811–1814
3 Dambrine, G., Cappy, A., Heliodore, F., and Playez, E.: 'A new method for determining the FET small-signal equivalent circuit', *IEEE MTT-S Int. Microw. Symp. Dig.*, 1988, 36, (7)
4 Golio, J.M.: 'Microwave MESFETs and HEMTs' (Artech House, 1991)
5 Ardaravicius, L., Matulionis, A., Liberis, J., Kiprijanovic, O., Ramonas, M., Eastman, L.F., Shealy, J.R., and Vertiatchikh, A.: 'Electron drift velocity in AlGaN/GaN channel at high electric fields', *Appl. Phys. Lett.*, 2003, 83, (19), pp. 4038–4040

Transform-limited optical pulses from 18 GHz monolithic modelocked quantum dot lasers operating at ~1.3 μm

M.G. Thompson, K.T. Tan, C. Marinelli, K.A. Williams, R.V. Penty, I.H. White, M. Kuntz, D. Ouyang, D. Bimberg, V.M. Ustinov, A.E. Zhukov, A.R. Kovsh, N.N. Ledentsov, D.-J. Kang and M.G. Blamire

18 GHz passive modelocking with Fourier-transform-limited optical pulses in InGaAs/GaAs quantum dot lasers emitting at ~1.3 μm has been achieved for the first time. An upper limit of 600 fs is estimated for the root-mean-square timing jitter (2.5–50 MHz).

Introduction: Quantum dot (QD) lasers were predicted [1] very early on to have superior performance as compared to conventional quantum-well lasers. A considerable number of advantages [2] have been realised such as ultra-low threshold current densities [3, 4], suppressed beam filamentation [5, 6] and low wavelength chirp and alpha parameter [6, 7]. Modelocking is a technique that can be used to overcome the electrical bandwidth limitations of laser diodes and achieve pulse generation at repetition rates far in excess of those obtained by direct modulation [8]. Monolithic modelocked laser diodes are desirable as they are compact, mechanically stable sources of picosecond optical pulses suitable for numerous photonic applications [9]. The reduced wavelength chirp of QD lasers makes them particularly attractive for achieving Fourier-transform-limited pulses under modelocking operation. However, to date, Fourier-transform-limited pulse generation in modelocked QD laser has not been reported. Previously we have demonstrated 10 GHz passive and hybrid modelocking in quantum dot lasers emitting at 1.1 μm [10]. However, in this Letter we show for the first time Fourier-transform-limited optical pulse generation in 18 GHz passively modelocked QD lasers, emitting at 1.3 μm.

Device description: The devices used for this study were grown on a GaAs:Si substrate by molecular beam epitaxy (MBE). The active region consists of a ten-layer stack of InAs quantum dots covered by 5 nm $In_{0.2}Ga_{0.8}As$. This was embedded in a GaAs waveguide and optical confinement was attained through an upper and a lower $Al_{0.75}Ga_{0.25}As$ cladding layer. Chemical wet etching was used to define 24 μm-wide shallow ridge waveguide structures. SiO_2 provided electrical isolation and Ti/Pt/Au formed the *p*-type contacts. As-cleaved lasers with a cavity length of 2.2 mm typically exhibit threshold current densities of 170 A cm^{-2} and a peak lasing wavelength of 1290 nm.

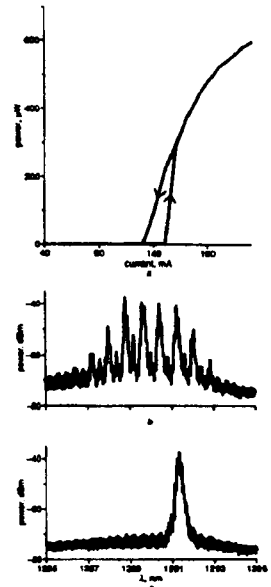


Fig. 1 *Hysteresis L-I and wavelength emission spectra*
a Hysteresis *L-I* with 'open-circuit' absorber
b Wavelength emission spectra under CW conditions
c Wavelength emission spectra under modelocking conditions

A ~130 × 5 μm trench was etched using a focused ion beam (FIB) to split the *p*-contact and define a 1600 μm gain section and a 600 μm-long absorber (consisting of two 300 μm-long sections). During the FIB processing, the inter-contact resistance, R_A, was monitored and the etch was stopped when R_I reached 1–2 kΩ. This allowed us to achieve sufficient electrical isolation between the laser sections without inducing significant damage. Hysteresis and bistability were observed in the *L-I* due to the nonlinear QD saturable absorber (Fig. 1*a*), even when the contact to the absorber section was 'open-circuit'.

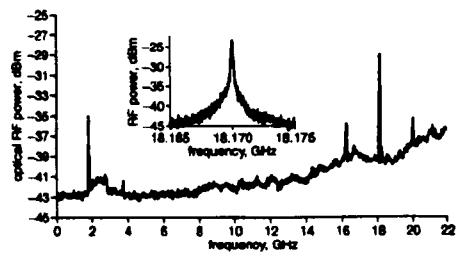


Fig. 2 *RF power spectrum under modelocking*
Inset: Close-in of 18.2 GHz peak

ARTICLE IN PRESS

Available online at www.sciencedirect.com

SCIENCE DIRECT®

Solid-State Electronics xxx (2004) xxx–xxx

SOLID-STATE ELECTRONICS

www.elsevier.com/locate/sse

Gallium nitride: the promise of high RF power and low microwave noise performance in S and I band

C.H. Oxley *

Engineering Technologies Research, De Montfort University, The Gateway, Leicester LE1 9BH, UK

The review of this paper was arranged by Prof. S. Cristoloveanu

Abstract

Gallium nitride (GaN) high electron mobility transistors (HEMT) promise very high RF output power density per unit gate periphery, which has been experimentally verified in a number of publications, for example 11.2 W/mm at 8 GHz published by the University of Cornell [Compd. Semicond. 7 (2001)], Research workers [Electron. Lett. 36 (2000) 469, IEEE Trans. Electron Device. 48 (2001) 581, IEEE Trans. Electron Device.] have also shown that the GaN HEMT will give surprisingly low microwave minimum noise figures (NF_{min}). The publications also suggest that the minimum noise figure plotted as a function of frequency can behave in quite different ways. This paper will present a simple analytical discussion on the reasons for the different minimum noise versus frequency behavior. The work will also compare the noise performance trends with the Indium Phosphide (InP) metaphorphic HEMT, and briefly discuss the performance limitations of the GaN HEMT. Finally, the work indicates the feasibility of a low microwave noise, sub 0.3 dB (NF_{min}) in I-band (8 –12.4 GHz), with a high drain gate breakdown voltage.

Keywords: Gallium compounds; MODFETs; Semiconductor device noise; Noise generators

1. Introduction

Gallium nitride has a number of properties, which make it very interesting compound semiconductor for high frequency high power transistors. In particular the avalanche breakdown field (E_{dc}) is in excess of 330 MV/m, almost 10× higher than for gallium arsenide (GaAs), enabling a much greater voltage swing across the output of the transistor, resulting in considerably higher RF output power density per millimeter of gate periphery. Recent experimental results for aluminum gallium nitride/gallium nitride (AlGaN/GaN) HEMT have shown output powers in excess of 11.2 W/mm [1] compared with 1 W/mm for GaAs [5] at 8 GHz. Monte-Carlo simulations [6] indicate that the material also offers a high saturated electron velocity (v_s) compared with GaAs, giving the potential of high unity-gain cut-off frequency, (f_t). This puts the material in a good position for the design of high power RF/microwave transistors. It is therefore not surprising that the main research/development thrust has been aimed at the medium/high power market.

Recently, published results [2–4] from a number of organizations, have shown that respectable microwave minimum noise figures can also be obtained from AlGaN/GaN HEMTs, for example 0.42 dB at 8 GHz [3] and with a high gate breakdown voltage (V_{gd}), in excess of 47 V. The publications show that when NF_{min} is plotted against frequency, a number of profiles have been found, including flat [3,7] and linear responses [4] with increasing frequency. One publication contained a departure, in which the experimental NF_{min} when linearly extrapolated intersected the frequency axes at approximately 6 GHz [3]. This is a surprising result as it suggests the feasibility of a very low noise figure in C-band. All the published noise results indicate that the transistors

* Fax: +44-116-250-6158.
E-mail address: choxley@dmu.ac.uk (C.H. Oxley).

0038-1101/$ - see front matter © 2004 Published by Elsevier Ltd.
doi:10.1016/j.sse.2004.02.005

have a very high breakdown voltage compared with GaAs. This will make them an interesting contender to GaAs or InP based transistors in some low noise front-end applications where limiter diodes would normally be required. This paper will attempt to explain the different minimum NF_{min} behavior with frequency, and then compare with published NF_{min} data for the InP metamorphic HEMT [8].

1.1. Discussion on microwave transistor noise

There is no naturally occurring crystal of GaN and therefore it has to be grown on a substrate of different material, which will introduce a lattice mismatch. There will also be significant differences in the thermal expansion coefficient (TEC) which will cause bowing of the substrate. These effects will introduce bulk and surface defects into the semiconductor between the gate and drain electrodes of the transistor. The defects will have a significant effect upon the microwave performance of the transistor, for example giving rise to dispersion effects [9] in the IV characteristics, this is already an area of research in GaN power transistors. The material defects will influence other transistor parameters, for example the *cut-off* frequency, and the output conductance (g_{ds}).

To investigate the effect these transistor parameters have on the intrinsic noise sources of a GaN HEMT (Fig. 1) and subsequently the minimum noise figure as a function of frequency; a very simple analytical approach has been adopted, based on the published work of Pucel [10], Cappy [11], and Shin [12].

To simplify the discussion, only the intrinsic noise performance will be investigated, therefore the thermal noise contribution from the extrinsic source resistance (R_s), and gate resistance (R_g) will be neglected.

The minimum noise figure for an intrinsic FET [10], neglecting the higher order terms is given by:

$$NF_{min} = 1 + 2(f/f_t)[PR(1 - C^2)]^{0.5} \quad (1)$$

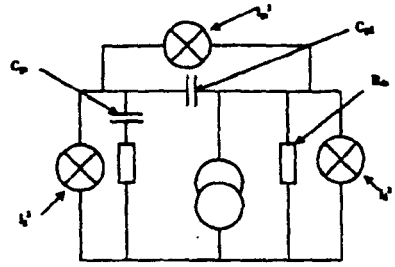


Fig. 1. Schematic noise model of the intrinsic HEMT.

P = drain noise coefficient; R = gate noise coefficient; C = noise correlation coefficient

The above expression does not take into account the capacitive coupling between the gate and drain (C_{gd}), or the gate leakage (I_{gs}) due to semiconductor surface defects and the high electric fields between the gate and drain electrodes.

The noise coefficients P and R can be calculated using Van der Ziel [13] formulation of the square of the drain and gate noise currents respectively in a bandwidth Δf which are given by the expressions $P = \langle i_d^2 \rangle / 4kTg_{ms}\Delta f$, $R = \langle i_g^2 \rangle g_{ms}/4kT\Delta f C_{gs}^2\omega^2$ and the correlation factor $C = \langle i_g \rangle \cdot \langle i_d \rangle / (\langle i_g^2 \rangle \cdot \langle i_d^2 \rangle)^{0.5}$, where T is the temperature of the channel °K, g_{ms} is the intrinsic transconductance, C_{gs} the gate source capacitance and ω the angular frequency. To evaluate the minimum noise figure at a specific bias point the parameters P, R and C are determined. The drain noise (i_d^2) is normally the most significant of the noise sources and is dependent on the channel diffusion current. From Eq. (1) it is seen that the gate noise (i_g^2) influences the drain noise (i_d^2) even at very low frequencies as the two noise sources are correlated. Therefore, under optimum bias conditions, a reduction in $\langle i_d^2 \rangle$ is expected which is determined by the magnitude of the correlation factor C. As the parameters P, R and C are biased dependent the NF_{min} remains linearly dependent on frequency [10]. The physical mechanism for the generation of the gate noise is uniform due to the direct correlation with the noise sources within the channel. However, if gate noise is generated, for example by leakage effects at the surface of the semiconductor extra noise will be generated within the device which will not be correlated, and therefore will not influence C the correlation factor or the induced gate noise.

Published parameters for R and C at the low noise bias condition and at the onset of saturation for a GaAs device are $R = 0.5$ and $C = 0.9$ [11], while recent work by Lee [7] suggests for GaN device $R = 0.5$ and $C = 0.7$.

Delagebeaudeuf [13] showed that it is a reasonable approximation to take the diffusion coefficient D, parallel to the electric field under the gate, as the constant low field value $D \approx kT_0\mu/q$, and assume the perpendicular diffusion coefficient D is zero, where μ is the low field carrier mobility and q the electronic charge.

By considering that the transistor is biased to the knee point (V_k) and the critical field (E_c) is at the edge of the gate nearest the drain, the mobility under the gate is a constant and an expression for P can be found

$$P = I_{ds}/(g_{ms}E_cL_{eff}) \quad (2)$$

The simple approximation can be expressed as the spectral density $S_{id}(f) = 4kTg_{ms}P$ A²/Hz, and has been shown to give reasonable agreement with measured values for GaAs based transistors [14].

The band structure for GaN is more complex than GaAs, giving a complicated velocity–field V–E characteristic, which to a first order can be represented by a piece-wise model see Fig. 2. It is well known that strain will reduce the band-gap [15] and high levels of defects will substantially modify the internal electric field [15] within the semiconductor. Couple this with the possibility of large gate-fringing and self-heating effects, the actual 'device' V–E characteristic could be substantially modified, and to a first approximation represented by the dashed line in Fig. 2. In the low field region the mobility of un-doped GaN at room temperature is of the order of 1100 V s cm^2 [3], giving rise to a saturation velocity around 10^7 cm/s, which is similar to experimental values observed by a number of workers [16]. The typical knee-voltage for a GaN HEMT is 4–5 V, and with a nominal source drain spacing of 3.0 μm, the electric field parallel with the gate will be of the order of 20 kV/cm, shown in Fig. 2. Recent published work [17] has shown that the drift velocity can saturate at low fields typically 15–20 kV/cm, and is thought to be partially due to self-heating effects within the transistor.

Using the above results and for a 0.41 μm gate-length HEMT, $S_{id}(f) = 6.64 \times 10^{-22}$ A^2/Hz which agrees well with an experimentally measured value of 4.0×10^{-22} A^2/Hz, published by the University of Cornell [7]. It is interesting to note that for a similar geometry device fabricated on GaAs, $S_{id}(f) = 2.3 \times 10^{-21}$ A^2/Hz.

With increasing frequency the experimental NF_{min} of GaAs transistors is seen to depart from the linear frequency response [18]. Cappy [11] has shown that this can be partly or wholly attributed to the gate-drain feedback capacitance, which effectively makes the drain current noise source frequency dependent.

$$\langle i_{dn}^2 \rangle = \langle i_{d0}^2 \rangle [1 + (f/f_0)^2] \tag{3}$$

where $f_0 = \{g_{ds}(V_{gs}, V_{ds})/2\pi C_{gd}(V_{gs}, V_{ds})\}$ and therefore will be dependent on the bias point, where V_{gs} and V_{ds} are the gate source and drain source voltages respectively.

Combining Eqs. (2) and (3) a more complete expression for P can be obtained

$$P = [I_{ds}/g_m E_s L_{eff}][1 + (f/f_0)^2] \tag{4}$$

Provide $f < f_0$ then P is frequency independent, and above $f_0 P$ becomes frequency dependent and will be a function of gate-length and the quality of the buffer layer and interfaces.

If the device is operating in the saturation region beyond the knee point, then $g_{ds} \approx 2\varepsilon' \varepsilon_0 W b_{saturation}/kL_{eff}$ and $C_{gd} \approx L_{eff} W \varepsilon_0/\varepsilon$.

Where W = total active width of the transistor, ε' = relative dielectric constant of the buffer layer, ε = relative dielectric constant of the active layer, $v_{saturation}$ = carrier saturation velocity in the buffer layer, and b is the depletion width. The term k is a factor relating the effective gate-width L_{eff} to the thickness of the buffer layer. For GaAs devices $k \approx 1/3$ and this was assumed for GaN although in reality it will be >1/3 because of the inferred larger effective gate-length due to the higher electric fields. The above assumption is made on the basis that the total width of the transistor is active. If, however, the width of the transistor is a single-stripe and its length increased, the resistive contribution increases and at a predetermined frequency only part of the width will be active [19], therefore the 'effective' depletion layer depth a will decrease. This will result in reducing K and therefore f_0. Hence, transistors of a given gate-length with a large unit gate-width (w_{unit}) will have a lower f_0, which has been experimentally observed [18].

$$f_0 \approx v_{saturation} K \varepsilon'/(\pi \varepsilon L_{eff}^2) \quad \text{and} \quad K(w_{unit}) = a/k \tag{5}$$

To a first approximation f_0 is increased, by reducing the gate-length and the unit gate-width to maintain a low gate resistance and assuming the carriers have reached saturation in the buffer region.

In reality f_0 is determined by de-embedding the intrinsic values of C_{gd} and g_{ds} from the measured s-parameters of a given transistor structure.

A recently published paper by Shin [12] has included gate leakage currents I_g as an additional shot noise source $\langle i_{gn}^2 \rangle = 2qI_g$ between the gate and drain contacts. This noise originates due to the reverse leakage current of the Schottky barrier at the high electric field region near the drain contact, high surface defect densities and poor metal to semiconductor interfaces. The spectral density of the shot noise source is $S_{ig}(f) = 2qI_g$, and typically $<10^{-23}$ A^2/Hz. Provided that $S_{ig}(f) \ll S_{id}(f)$,

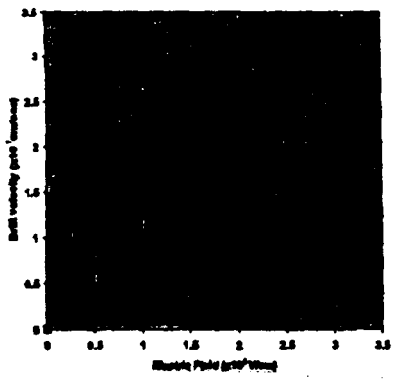


Fig. 2. Piece-wise model for the velocity–field characteristic of gallium nitride.

and higher order terms are neglected, Shin [12] derived the following expression for NF_{min}:

$$NF_{min} = 1 + 2f/f_t\sqrt{(PR_s)}[1 + (f_a/f)^2]^{0.5} \quad (6)$$

Assuming $R_i \approx 1/(2g_{ml})$, then to a first approximation $f_a = f_t\{2qI_{gs}/[g_{ml}^2kT]\}^{0.5}$.

Combining Eqs. (6) and (4) gives the minimum noise figure NF_{min} as

$$NF_{min} \approx 1 + 2(f/f_t)\{[I_{ds}/2g_{ml}L_gL_{ds}][1 + (f/f_0)^2][1 + (f_a/f)^2]R[1 - C^2]\}^{0.5} \quad (7)$$

For the purpose of this work the induced gate current will be considered to be zero.

1.2. Device DC and RF measurements

To investigate the effects of f_0 and f_a on the performance of the GaN HEMT the variation of g_m, C_{ds}, and I_g with bias voltage (V_{ds} and V_{gs}) were experimentally determined. It was assumed that the behavior of the s-parameters is similar for all AlGaN/GaN HEMT's, and the device will follow the standard scaling rules.

An AlGaN/GaN HEMT transistor was fabricated at the QinetiQ facility in the UK. The transistor consisted of a nominal 0.25 μm gate-length with a metallised 'T' profile to minimise the gate resistance (R_g), and the gate to drain spacing was nominally 2 μm. The total gate-width was 0.1 mm and consisted of two gate fingers each 0.05 mm in width. The structure was fabricated on a SiC substrate with an AlN buffer region and the transistor surface was passivated with silicon nitride (Si_3N_4). The small-signal s-parameters were measured by QinetiQ over a wide range of bias conditions and from 0.25 to 50 GHz using an Agilent network analyser and RF probe station. The device was found to have a pinch-off voltage (V_p) of −6.5 V and a maximum cut-off frequency (f_t) of 37 GHz when biased with $V_{gs} = -6$ V.

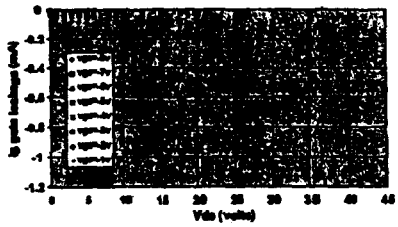


Fig. 3. Gate leakage I_g as a function of V_{ds} and V_{gs}.

The dc gate leakage was plotted as a function of V_{ds} and V_{gs}, and is shown in Fig. 3. The knee voltage of the device was approximately 5 V, the saturation current (I_{dss}) approximately 130 mA and the maximum intrinsic transconductance of 28 mS. Fig. 3 shows for a V_{gs} approaching pinch-off, the gate leakage current will increase rapidly with V_{ds}. As pinch-off is approached, the operating current is between 10% and 15% I_{dss} which is close to the bias point for low noise operation [20].

The intrinsic parameters of the small-signal equivalent circuit model were obtained, by de-embedding from the measured small-signal s-parameters [21]. It was found necessary to de-embed the gate-source (R_{gs}) and drain gate (R_{dg}) leakage resistances. The intrinsic output resistance R_{ds} was plotted as a function of V_{gs} and V_{ds} as shown in Fig. 4. The output conductance $g_{ds} = 1/R_{ds}$.

Fig. 4 shows that when the device is pinched-off, R_{ds} reduces with increasing V_{ds}, indicating that carriers are being generated within the buffer interface layer. As V_{gs} is increased R_{ds} increases with V_{ds}, unlike the InP metamorphic HEMT where R_{ds} still decreases. The decrease in R_{ds} in the metamorphic HEMT was explained by the onset of impact ionization, which lead to a further source of noise in the channel. Therefore it appears safe

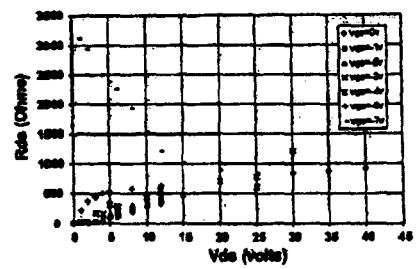


Fig. 4. R_{ds} versus V_{ds} for different V_{gs}.

to assume that in the GaN HEMT this noise source can be neglected. From Fig. 4 saturation in R_{ds} appears to occur when V_{ds} is in excess of 15 V. Therefore within the operating region of the device the magnitude of R_{ds} will be dependent on the DC operating point. For example, at V_{ds} of 5 V and for a V_{gs} approaching pinch-off, $g_{ds} \approx 2.0$ mS. Whereas in saturation $V_{ds} = 20$ V, $g_{ds} \approx 1.25$ mS.

Separate measurements on a 0.9 μm gate-length AlGaN/GaN HEMT has shown $g_{ds} \approx 6.6$ mS in the saturation region, and assuming the carrier mobility in the buffer layer is small [22], then to a first approximation g_{ds} appears to scale with the effective gate-length L_{eff}.

The measured intrinsic gate drain feedback capacitance and drain source conductance for different V_{ds} and V_{gs} were used in the expression $f_0 = g_{ds}/2\pi C_{gd}$; f_0 was calculated and plotted as a function of V_{ds} and V_{gs} in Fig. 5. The plot indicates that at low V_{ds} there is considerable variation in f_0 depending on the gate bias V_{gs} setting. It should be noted that C_{gd} is dependent on the semiconductor material, thickness of the passivation layer, and device geometry including the gate metallisation profile, depth of recess, and the gate drain spacing. Therefore C_{gd} can vary considerably from device structure to device structure.

1.3. Comparison between simple model and published measured NF_{min} trends, at different bias conditions

The simple analytical model and the de-embedded device parameters, were used to investigate the different NF_{min} versus frequency responses, which have appeared in the published literature. Consider a device with a 0.25 μm gate-length, a unit gate-width of 0.05 mm, giving a total gate-width of 0.1 mm and a nominal gate drain spacing of 2 μm and a mounted f_t of 37 GHz. The transistor was biased at $V_{ds} = 15$ V and $V_{gs} = -6$ V, the estimated operating current and gate leakage will be approximately 25 mA and 50 μA, respectively. The operating values for g_{ds} and C_{gd} are assumed to be 1.5 mS and 0.014 pF, respectively. The calculated NF_{min} versus frequency is shown in Fig. 6.

If the f_t of the transistor is increased to 75 GHz by reducing the gate-length, and assuming perfect scaling of the intrinsic transistor parameters, it is found that the gate leakage has a greater influence on the NF_{min} performance versus frequency. This behavior is also shown in Fig. 6 and is similar in behavior to the experimental results published in [3].

Now consider the 0.25 μm gate-length transistor is operated at a very low V_{ds}, less than 5 V and relatively close to pinch-off, giving an I_{ds} of <10 mA (≈10% I_{dss}) and assume the f_t of the device remains at 37 GHz. As the device is operated at a low V_{ds} and relatively close to pinch-off the gate leakage current is small, of the order 5 μA. Values of g_{ds} and C_{gd} are assumed to be 2.0 mS and 0.018 pF, respectively. The NF_{min} versus frequency is given in Fig. 7 and is linear in behavior and showing a similar trend to the published data in [4].

Lastly, assume the same 0.25 μm gate transistor has a unit gate width of 100 μm giving a total gate-width of 200 μm and the gate drain spacing is reduced to approximately 1 μm. These geometrical changes will

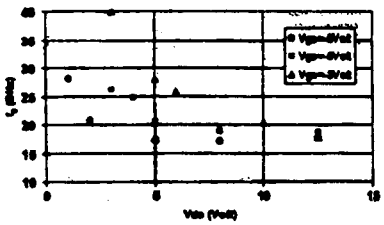


Fig. 5. 'f_0' as a function GaN HEMT bias.

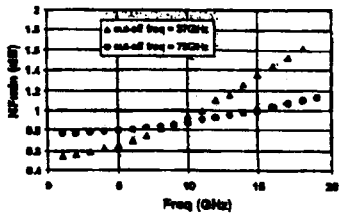


Fig. 6. The calculated NF_{min} of a GaN HEMT versus frequency with a gate leakage current of 40 μA, and f_t approx 18 GHz.

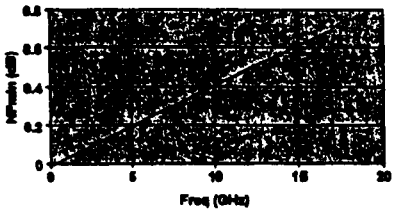


Fig. 7. NF_{min} versus frequency for device operating at low V_{ds}. Low gate leakage and high $f_t > 25$ GHz.

reduce f_0. Using previously published experimental data [18] it appears f_0 may be reduced by a factor of approximately 1.4, by increasing the unit gate-width from 50 to 100 μm. Further reduction in f_0 would also be expected if the gate drain spacing was reduced. Therefore, a f_0 of approximately 11 GHz was assumed and the transistor biased at $V_{gs} = -5$ V and $V_{ds} = 6$ V the gate leakage was assumed to be 10 μA, and the operating current 20% of I_{dss}.

Using Eq. (1) the intrinsic noise of the transistor can be calculated, and is plotted in Fig. 8. Interestingly the NF_{min} performance of the 0.2 mm gate-width device when extrapolated back to the frequency axis, intersects the axis at around 4 GHz which is similar in behavior to the measured noise performance of a GaN HEMT published by Nguyen [2]. The simulated and experimental NF_{min} performance indicates that it may be feasible to design a GaN transistor with exceptionally low NF_{min} in S to I-bands and retain the high drain gate breakdown voltage.

The simple analytical model shows that provided the correct choice of unit gate-width is made then the different published NF_{min} versus frequency can be explained by the bias operating point of the GaN HEMT which will partly determine the leakage current and output conductance. These two parameters will have an effect upon the behavior of NF_{min} with frequency. Similar effects have been published for the InP metaphorphic HEMT and were reported to be due to impact-ionization [8]. However there are some differences. When the InP metaphorphic HEMT is biased at a high V_{ds} the NF_{min} initially decreases before flattening out and then increases with frequency. At low V_{ds} the frequency response is linear and very similar to Fig. 7. These effects were explained by the inclusion of a current noise source as a function of g_{ds} in parallel with the channel. The origin of this noise source was described by the impact ionization increasing the number carriers and therefore increasing the channel conductance as V_{ds} increased. Whereas, for the GaN HEMT the NF_{min} increases with frequency, which agrees with a decreasing g_{ds} with increasing V_{ds} for all operating V_{gs}. The performance limitation of the GaN device is thought to be due to increasing gate-leakage.

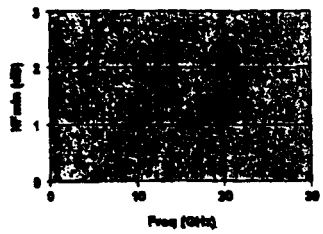


Fig. 8. NF_{min} as a function of frequency with low 'f_0' of approximately 11 GHz.

2. Conclusions

The simple analytical approach explains the differences seen when operating the GaN HEMT at high and low V_{ds} bias settings. At high V_{ds} voltages the gate drain leakage current substantially increases leading to an increase in NF_{min} and a flattening of the response with frequency. At low V_{ds}, f_0 rapidly decreases before beginning to saturate at high V_{ds} thus effecting the high frequency response of NF_{min}. The increasing leakage current appears not to be a function of g_{ds}, which suggests that it is surface related.

Therefore, improvements in noise performance may be expected with increased understanding of the surface properties of GaN [23]. The simple analytical model also suggests the possibility of obtaining very low minimum noise figures in S and I band by careful geometrical design of the device and operating at a low V_{ds} to minimise noise caused by current leakage effects.

The work also indicates that the correct choice of unit gate-width must be made in order to maintain the high frequency response of NF_{min}, otherwise anomalous looking NF_{min} versus frequency profiles may be obtained.

Acknowledgements

The author acknowledges that the work was partially supported by MOD and EPSRC on the grant GR/R21073. The author also acknowledges M. Uren and D. Hayes of QinetiQ for the supply of *s*-parameter measurements of nominal 0.25 μm gate-length GaN HEMT, and would like to thank Electronic and Electrical Engineering Department of DeMontfort University, Leicester, UK for enabling the work to be carried out.

References

[1] Eastman L. GaN reaches new power levels. Compd Semicond 2001;7(10).
[2] Nguyen NX, Micovic M, Wong WS, Hashimoto P, Janke J, Harvey D, et al. Robust low microwave noise GaN MODFETs with 0.6 dB noise figure at 10 GHz. Electron Lett 2000;36:469–71.
[3] Lu W, Yang M, Asif Khan, Adesida I. AlGaN/GaN HEMTs on SiC with over 100 GHz f_t and low microwave noise. IEEE Trans Electron Device 2001;48:581–5.
[4] Lu W, Kumar V, Piner E, Adesida I. DC, RF, and microwave noise performance of AlGaN/GaN field effect

transistors dependence of aluminium concentration. IEEE Trans Electron Devices.
[5] Wolaxi CA. RF power devices for wireless communications. MTTS Proc 2002:285–8.
[6] Bhatkar UV, Shur MS. Monte Carlo calculations of the velocity–field characteristics of Wurtzite GaN. J Appl Phys 1997;24(4):1649–55.
[7] Sangjae L, Vinayak T, Webb K, Eastman LF. Intrinsic noise characteristics of AlGaN/GaN HEMTs. IEEE MTTS 2002:1415–8.
[8] Marsi MR, Lasker J, Nuttinck S, Raghavan A, Bergman JT, Eastman R, et al. Temperature-dependent small-signal and noise parameter measurements and modelling on InP HEMTs. IEEE Trans MTT 2000;48(12).
[9] Wu Y, Kapolnek D, Ibbetson J, Parikh P, Keller B, Mishra U. Very-high power density AlGaN/GaN HEMTs. IEEE ED 2001;48(3).
[10] Liechti CA. Microwave field-effect transistors-1976. IEEE Trans MTT 1976;24(6):279–300.
[11] Cappy A. Noise modelling and measurement techniques. IEEE Trans Microwave Theory Tech 1988;36(1):1–10.
[12] Shin D et al. Analytical noise model with the influence of shot noise induced by gate leakage current for submicrometer gate-length high electron mobility transistors. IEEE ED 1997;44(11).
[13] Dabgabanadeef D, Cherrier J, Laviron M, Duischene P. A new relationship between the Pukni coefficient and optimal current value for low noise operation of field-effect transistors. IEEE Electron Device Lett 1985;EDL-6(9).
[14] Folks P. Thermal noise measurements in GaAs MESFETs. IEEE Trans ED 1985;(6):620–2.
[15] Nevarmann P, Wolff I. Simulation of temperature dependencies using a new and CAD suitable physical GaAs MESFET model including the electron preheating effect. IEEE, MTTS 1995:931–4.
[16] Kumar V, Lu W, Schwindt R, Kuliev A, Simin G, Yang J, et al. AlGaN/GaN HEMTs on SiC with f_t of over 120 GHz. IEEE Elec Device Lett 2002;23(8):455–7.
[17] Ardaravicius L, Matulionis A, Liberis J, Kiprijanovic O, Ramonas M, Eastman LF, et al. Electron drift velocity in AlGaN/GaN channel at high electric fields. Appl Phys Lett 2003;83(19):4004–38.
[18] Oxley CH, Holden A. Simple models for high-frequency MESFETs and comparison with experimental results. IEE Proc 1986;133, Pt. H, p. 335–40.
[19] Liu W. Fundamentals of III-V Devices HBTs, MESFETs and HFETs/HEMTs. John Wiley and Sons Inc.; 1999.
[20] Oxley CH. A simple approach for calculating the minimum noise figure of GaN HEMTs which include gate leakage. Microwave Opt Technol Lett 2001;33(2).
[21] Dambrine G, Cappy A, Heliodore F, Playez E. A new method for determining the FET small-signal equivalent circuit. IEEE Trans MTT 1988;36(7):1151–9.
[22] Ishi SC, Wilander M, Narayan J, VanOverstraeten. III-nitrides: growth, characterization and properties. J Appl Phys 2000;87(3):965–1006.
[23] Tan WS, Houston PA, Parbrook PJ, Hill G, Airey RJ. Comparison of different surface passivation dielectrics in AlGaN/GaN heterostructure field-effect transistors. J Phys D; Appl Phys 2002;35:595–8.

PERGAMON

Solid-State Electronics 45 (2001) 677–682

SOLID-STATE ELECTRONICS

Calculation of minimum noise figure using the simple Fukui equation for gallium nitride (GaN) HEMTs

C.H. Oxley *

Emerging Technologies Research Centre, De Montfort University, The Gateway, LE1 9BH, Leicester, UK

Received 3 November 2000; received in revised form 31 January 2001; accepted 8 February 2001

Abstract

The aim of the paper is to present a simple noise model using the Delegedeundeauf formulation for the Fukui constant K_F, in order to estimate the minimum noise figure of Gallium nitride (GaN) based MESFET/HEMT devices. The Fukui model is compared with published experimental results of a 0.15 μm gate-length GaN HEMT and shows good agreement with the measured minimum noise figure between 5 and 26 GHz. The work indicates that with an improved F_t, which is dependent on material quality, very low noise figures of 0.4 dB at 12 GHz may be feasible from a GaN HEMT. © 2001 Elsevier Science Ltd. All rights reserved.

Keywords: Gallium nitride (GaN) HEMT; Noise figure; Fukui

1. Introduction

The possibility of using GaN high electron mobility transistors (HEMTs) in low noise front ends with the advantage of the high drain gate breakdown voltage (an order of magnitude greater than GaAs and Indium phosphide (InP)) would eliminate the need for additional protection circuitry in many applications [1].

To date there has been little published work to optimise the GaN transistor geometry for low noise operation. The Fukui equation provides a useful semi-empirical expression for estimating the room temperature minimum noise figure (F_{min}) of a GaAs field effect transistor (MESFET) operating at frequencies below which the reactive elements (for example C_{gd} gate/drain feedback capacitance) couple with the drain circuit [2]. The Fukui model assumes no intrinsic noise contribution from the gate circuit and therefore this equation can only be used to obtain an insight to the minimum noise performance and as a starting point for the optimisation of the device structure. The Fukui equation is given in Eq. (1):

$$F_{min} = 10 \log\left\{1 + \frac{K_F P}{F_t}\left[g_{mo}(R_g + R_s)\right]^{0.5}\right\} \text{ dB} \qquad (1)$$

where, F_{min} is the minimum noise figure (dB), F_t, the cut-off frequency (unity gain), F, the frequency of operation (GHz), g_{mo}, the intrinsic transconductance (mS), R_g, the gate resistance function of device geometry (Ω), R_s, the source resistance function of device geometry (Ω) and K_F, the empirical fitting factor. The fitting factor K_F, was originally derived experimentally for GaAs MESFETs and found to be ≈2.5 [2].

In this paper, the minimum noise performance curves with reference to frequency are derived for a GaN transistor. It is assumed that the electrical equivalent circuit model for the MESFET and HEMT are similar and differences arise only in the magnitude of the Fukui coefficient K_F which is largely determined by the material and the type of transistor (MESFET/HEMT).

2. Discussion

A relationship for K_F as a function of the optimum bias current, I_{opt}, for the minimum noise was derived for short gate-length transistors by Delegebeaudeauf et al. [3]. This expression is given Eq. (2) for completeness:

* Fax: +44-116-250-6473.
E-mail address: CHOXLEY@dmu.ac.uk (C.H. Oxley).

PII: S0038-1101(01)00069-7

23 B

$$K_T = 2\left(\frac{I_{opt}}{E_c L g_{mo}}\right)^{0.5} \quad (2)$$

where, I_{opt} is the optimum current (A) for minimum noise operation, L, the gate length (μm), g_{mo}, the intrinsic transconductance (mS) and E_c the peak velocity field (kV/cm).

Paper [3] also provides a comparison (for GaAs transistors) between the coefficient K_T derived from Eq. (2) and the corresponding experimentally derived value based on the measured minimum noise figure F_{min} and using Eq. (1). Good agreement was established and in general K_T was found to be smaller in magnitude for HEMT than for MESFET structures, and this was also substantiated in Ref. [4].

By combining Eqs. (1) and (2) a general expression for F_{min} can be derived as shown in Eq. (3), which is independent of the intrinsic transconductance, g_{mo}, and based on physical/measurable quantities for GaAs and GaN based transistors:

$$F_{min} = 10\log\left\{1 + \frac{2fL}{f_t}\left[\frac{I_{opt}(R_g + R_s)}{E_c L}\right]^{0.5}\right\} \text{ (dB)} \quad (3)$$

The cut-off frequency, can be estimated using $f_t = v_{sat}/(2\pi L)$ (neglecting any field fringing effects), where v_{sat} is the saturation velocity of the carriers, under the metallised gate of the transistor.

Therefore an estimate of the minimum noise figure of the transistor can be calculated using the following expression:

$$F_{min} = 10\log\left\{1 + \frac{4\pi fL}{v_{sat}}\left[\frac{I_{opt}(R_g + R_s)}{E_c L}\right]^{0.5}\right\} \text{ (dB)} \quad (4)$$

The Eq. (4) enables an estimation of the minimum noise figure in terms of material and device parameters.

In this paper Eq. (4) has been used to investigate the minimum noise figure behaviour of a GaN HEMT device with a range of gate lengths (0.15–0.25 μm), on the basis of the following assumptions:

In the calculation the critical velocity field E_c was assumed to be approximately 150×10^3 V/m, for a maximum peak velocity (3.2×10^5 m/s) at 300 K. These figures are derived from Monte Carlo analysis by Bhadkar and Shur [5]. More recent experimental work by Wraback and She [6] have suggested that the critical field figure may be higher (225×10^3 V/m) and the peak velocity lower (1.9×10^5 m/s) than the above theoretical calculations. These differences can be explained by high defect and trap densities in the device which maybe responsible for reducing the cut-off frequency f_t [7]. The saturation and peak velocities for GaN have been computed by a number of workers and these are summarised in Table 1, together with the experimental results of Wraback. The theoretical work of Bhadkar and Shur [5] also suggests that the peak/saturation velocity does not change significantly with the reduction of the carrier concentration from 10^{16} to 10^{18} atoms cm^{-3}. Therefore, from the theoretical results presented in Table 1, an average ratio of the theoretical saturation to peak velocities has been estimated as 0.62. Further, this value has then been used to calculate the corresponding saturation velocity from the experimental peak velocity. This gives a figure of 1.19×10^5 m/s which corresponds to a cut-off frequency of 76 GHz for a 0.25 μm gate length GaN transistor, and is consistent with the published maximum experimental cut-off frequencies measured for GaN devices [7]. The above figure for v_s has been used in the noise calculations and corresponds to the highest cut-off frequencies in the literature [7]. It is also interesting to note that the work of Bhadkar indicates a much smaller rate of change in the carrier velocities with temperature when compared with GaAs, which can perhaps result in improved noise figure characteristics over temperature.

Recent publications [8] on GaN HEMT transistors indicate that devices with a high extrinsic transconductance, g_{mo}, (250–300 mS/mm) have a peak current of the order of 1.2 A/mm. The optimum current I_{opt} for minimum noise figure, F_{min}, has been assumed to be ≈20% of $(I_{ds})_{max}$.

A range of total parasitic resistance values (5–40 Ω) representing the combined parasitic source and gate resistances $(R_s + R_g)$ is assumed. The actual values depend on the device geometry and material properties of the device. For example, the parasitic source resistance, R_s, is a function of the contact resistance,

Table 1

	Ref. [13]	Ref. [5] Monte Carlo	Ref. [11]	Ref. [12] Monte Carlo	Ref. [6] Experiment
Saturated velocity ($\times 10^5$ m/s)	2.2	2.5	1.5	1.6	1.19[a]
Peak velocity ($\times 10^5$ m/s)		3.2	2.7	2.9	1.9
Ratio sat/peak		0.78	0.55	0.55	0.62[a]
Critical electric field (kV/m)		150		200	225

[a] Derived from table data.

R_{sg}, the gate to the source contact separation, the gate/channel geometry (etched well etc.) and the mobility of the majority carriers in the material. The published mobility figure for electrons in GaN varies between 1200 and 2000 $cm^2/V s$ at 300 K [1,5]. The gate parasitic resistance, R_g, depends on the gate profile (T-profile) and metallisation thickness, as well as the number of unit gate stripes.

Fig. 1a and b show the calculated minimum noise figure F_{min} of a GaN HEMT, plotted as a function of frequency (5–30 GHz) for different values of the total combined parasitic source and gate resistance ($R_s + R_g$), for two gate lengths of 0.15 and 0.25 μm respectively. The plots indicate the feasibility of obtaining low noise figure even with high total parasitic resistance ($R_s + R_g$). For example, a 0.15 μm gate length GaN HEMT at

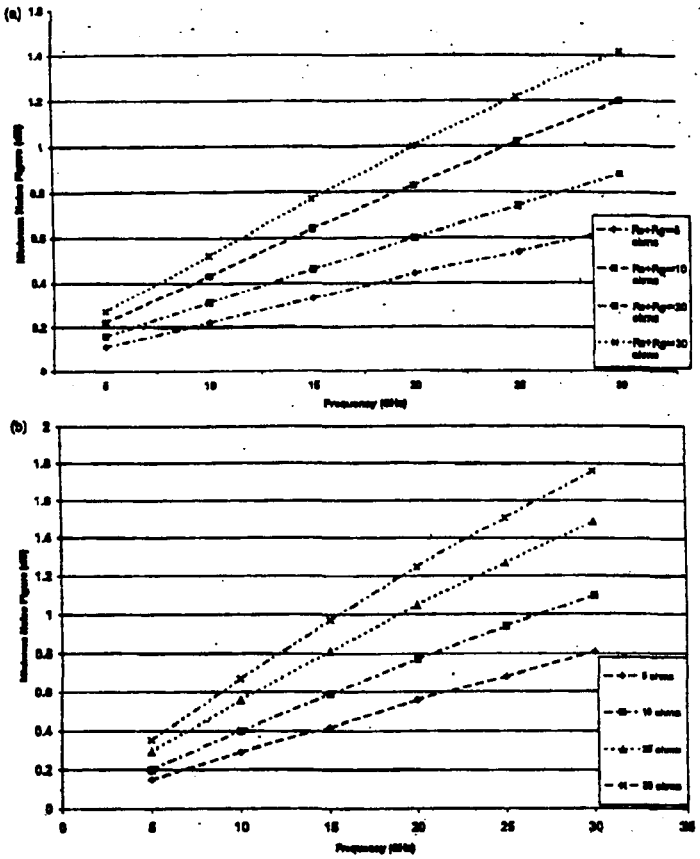


Fig. 1. (a) Minimum noise figure, for 0.15 μm gate length GaN HEMTs with different values of total parasitic resistance and (b) minimum noise figure, for 0.25 μm gate length GaN HEMTs with different values of total parasitic resistance.

30 GHz has a calculated F_{min} of 1.6 dB assuming a total parasitic resistance of 40 Ω.

In comparison the minimum noise figure has been calculated using Eq. (4) for a GaAs MESFET, with the following assumptions:

The critical electric field is assumed to be 3.5×10^6 V/m, with a saturation velocity of 10^5 m/s to give a cut-off frequency F_t of approximately 64 GHz for a device with a 0.25 μm gate length. An identical, device geometry has been assumed and the low noise optimum current at 20% of I_{dss} is ≈12 mA [9].

The experimental published work [10] suggests an estimated total measured parasitic resistance $(R_s + R_g)$ of between 5 and 8 Ω, for a SCALEO device of 200 μm total gate width. In Fig. 2 is shown the calculated minimum noise figure F_{min} for a 0.25 μm gate length GaAs MESFET, plotted against frequency (5–30 GHz) for different values of the total combined parasitic source and gate resistance. Good agreement between the published experimental results [10] of measured minimum noise figure values for a nominal 0.25 μm gate length MESFET and the calculated numbers for a total parasitic resistance $(R_s + R_g)$ of approximately 5 Ω is clearly evident.

To provide consistancy in the comparison between a GaN and GaAs HEMT, it is assumed that the R_g is identical for both GaN and GaAs devices and the major difference arises only in the value of source parasitic resistance R_s. The source resistance consists primarily of two parts the contact resistance, R_c and the resistance of the semiconductor. If R_c is identical for both devices, then R_s differs by approximately the ratio of the mobilities between GaAs and GaN. The bulk mobility in GaAs is approximately 8000 [11], which is a factor of 4–6.8 greater than that of GaN. Therefore the parasitic resistance R_s will be to a first order of approximation, four to seven times larger in the GaN device when compared with the GaAs device.

With reference to the experimental results for the 200 μm GaAs MESFET device at 20GHz, the F_{min} is 2.0 dB with a source resistance of approximately 0.75 Ω/mm [10]. A comparable GaN device, R_s is 3–5 Ω/mm, resulting in a noise figure of approximately 1.1 dB at 20 GHz. Interestingly, this result suggests that the GaN device even with a low mobility and higher parasitic source resistance, can still give a lower noise figure.

The published experimental measurements of Nyguyen [1] have been directly compared with the calculated results from the Fukui Eq. (4). A critical electric field of 150 kV/cm was assumed and the saturation ve-

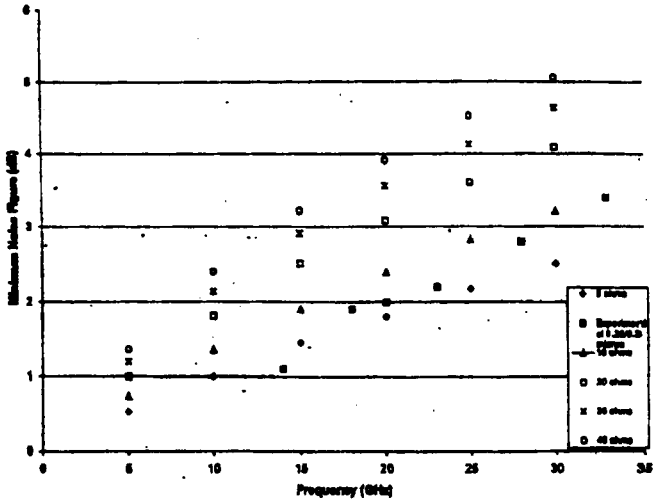


Fig. 2. Minimum noise figure, for 0.25 μm gate length GaAs MESFET with different values of total parasitic resistance and comparison with experiment.

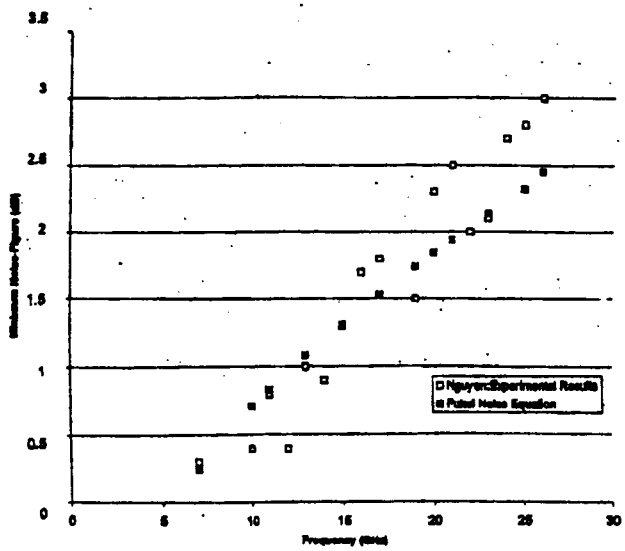


Fig. 3. Comparison between experimental and calculated minimum noise figure of a GaN HEMT to 26 GHz.

locity was estimated as 0.47×10^5 m/s from the measured F_t of 50 GHz [1] of the 0.15 μm gate length device; I_{opt} has been assumed to be 20% of 1.25 A/mm for a 0.2 mm total gate periphery [1]. The estimated combined $R_s + R_g$ of 35 Ω ($R_s = 26$ Ω, $R_g = 9$ Ω) includes the gate resistance contribution and source resistance. Fig. 3 shows good agreement between experimental and calculated minimum noise figure from 5 to 26 GHz. The experimental results also show an increase in minimum noise figure with increasing frequency when compared with the Pukui noise model. This discrepancy is to be expected as the simple linear Pukui model does not take into account the gate noise contribution or coupling due to the reactive elements becoming more significant with increasing frequency.

The presented work indicates that the simple Pukui model with the modification described can provide a good first order estimate of the noise performance for GaN MESFET/HEMT devices. It may be possible to extend the analyses to devices on other wide band gap materials. The model also suggests that further improvements in the minimum noise figure can be obtained by increasing the F_t of the device and optimising the geometry to minimise the parasitic resistances and therefore the thermal contribution to the noise generation. A high level of defects including traps and a high field fringing region extending well beyond the gate metallisation [12] are currently limiting the F_t to low value and therefore the full potential of the GaN device has yet to be realised.

3. Conclusions

A simple expression for deriving the noise figure of a GaN HEMT device is presented. The Pukui model fits well to available experimental data from 5 to 26 GHz. The simple expression suggests that lower noise figures (<0.3 dB at 10 GHz) may be feasible with GaN based devices provided the F_t is significantly improved.

Acknowledgements

The author would like to express his thanks to Dr. O. Buiu for assistance during the preparation of this paper (Dr. O. Buiu is now at the University of Liverpool) and

262